1. General Description

The LTD226X family are high-precision, multi-channel, 40-kSPS, delta-sigma (Δ-Σ) analog-to-digital converters (ADCs). Features, for example, programmable gain amplifier (PGA), precise and low-drift voltage reference, monitors for fault detection, general purpose input output options are included in this highly-integrated chip making it a single-chip solution to deal with measurements tasks such as weigh scales, resistance temperature detectors (RTDs) and thermalcouple sensors.

The main path of analog-to-digital conversion consists of an input multiplexer (5 channels for LTD2260 and 10 channels for LTD2261), a low-noise PGA, a 24-bit Δ-Σ modulator, a precise and low-drift voltage reference, and a programmable digital filter. The 1 GΩ high input impedance of the PGA minimizes the error induced by sensor loading. The device provide two individual current source with programmable supplying current, that simplifies the circuit of RTDs measurements.

The conversion is completed by a fourth-order Δ-Σ modulator combined with a flexible digital filter. The filter supports a simultaneous 50-Hz and 60-Hz rejection mode and single-cycle settling mode. Associated with internal signal and reference monitors, a temperature sensor and CRC data verification, the output data is more reliable.

The LTD226X family are available in 5 mm × 5 mm QFN packages and specified in temperature range from -40℃ to 125℃.

2. Features and Benefits

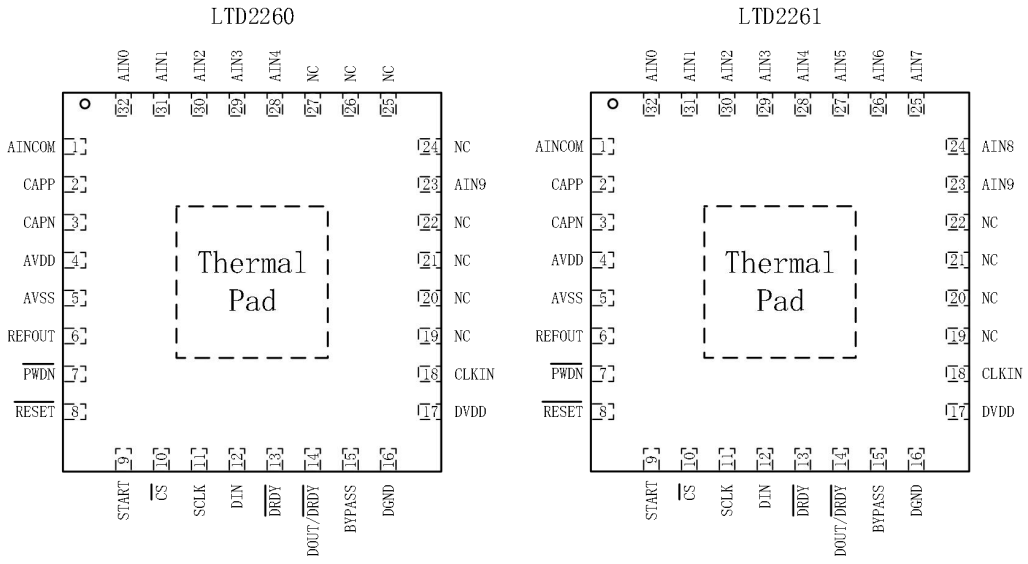
- High-precision, 24-bit delta-sigma ADC
- Low noise: 30 nVRMS (@20 SPS, gain=128)
- Linearity: 2 ppm
- 5 single-ended inputs or 3 differential inputs (LTD2260)
- 10 single-ended inputs or 5 differential inputs (LTD2261)
- PGA gain: 1 to 128
- Input voltage range: ±7 mV to ±5 V
- Data rate: 2.5 SPS to 40 kSPS
- Low drift 2.5 V reference: 2 ppm/℃
- Simultaneous 50-Hz and 60-Hz rejection mode
- Single-cycle settling mode
- PGA voltages and reference monitors
- 5 V or ±2.5 V supply
- Integrated temperature sensor
- Cyclic redundancy check
- Two individual current source
- Sensor burn-out detection
- 4 GPIOs available
- AC excitation for bridge sensors

- SPI compatible

3. Applications

- Temperature and pressure measurement
- Analog input modules in PLC and DCS
- Weigh scales and strain-gauge digitizers
- Scientific and lab instruments

4. Pin Configuration (Top View)



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6. Revision History

Version 0

Initial version.

7. Device Comparison

Part Number	Input Channels		Reference Inputs	GPIO AC Excitation
	Single-ended	Differential		
LTD2260	5	3	1	NA
LTD2261	10	6	2	4

8. Pin Description

Pin number	Pin Name		Description
	LTD2260	LTD2261	
1	AINCOM	AINCOM	Analog common input / IDAC1 / IDAC2 / VBIAS
2	CAPP	CAPP	PGA positive output. Connect a 4.7 nF C0G capacitor between CAPP and CAPN
3	CAPN	CAPN	PGA negative output. Connect a 4.7 nF C0G capacitor between CAPP and CAPN
4	AVDD	AVDD	Positive analog power supply input
5	AVSS	AVSS	Negative analog power supply input
6	REFOUT	REFOUT	Internal reference output. Connect a 10 µF capacitor to AVSS
7	$\overline{\text{PWDN}}$	$\overline{\text{PWDN}}$	Power down input. Active low
8	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	Reset input. Active low
9	START	START	Start conversion control input. Active high
10	$\overline{\text{CS}}$	$\overline{\text{CS}}$	SPI chip select input. Active low
11	SCLK	SCLK	SPI clock input.
12	DIN	DIN	SPI data input.
13	$\overline{\text{DRDY}}$	$\overline{\text{DRDY}}$	Data ready indicator output. Active low
14	DOUT/$\overline{\text{DRDY}}$	DOUT/$\overline{\text{DRDY}}$	SPI data output / Active-low data ready indicator output.
15	BYPASS	BAPASS	Internal regulator output. Connect a 1 µF capacitor to DGND
16	DGND	DGND	Digital ground
17	DVDD	DVDD	Digital power supply
18	CLKIN	CLKIN	Connect to DGND to use internal oscillator / External clock input
19	N.C.	N.C.	N.A.
20	N.C.	N.C.	N.A.
21	N.C.	N.C.	N.A.
22	N.C.	N.C.	N.A.
23	N.C.	AIN9	LTD2261 only: Analog input 9 / IDAC1 / IDAC2
24	N.C.	AIN8	LTD2261 only: Analog input 8 / IDAC1 / IDAC2
25	N.C.	AIN7	LTD2261 only: Analog input 7 / IDAC1 / IDAC2
26	N.C.	AIN6	LTD2261 only: Analog input 6 / IDAC1 / IDAC2
27	N.C.	AIN5	LTD2261 only: Analog input 5 / IDAC1 / IDAC2 / GPIO3 / ACX2
28	AIN4	AIN4	LTD2260: Analog input 4 / IDAC1 / IDAC2 LTD2261: Analog input 4 / IDAC1 / IDAC2 / GPIO2 / ACX1
29	AIN3	AIN3	LTD2260: Analog input 3 / IDAC1 / IDAC2 LTD2261: Analog input 3 / IDAC1 / IDAC2 / REFN1 / GPIO1 / $\overline{\text{ACX2}}$
30	AIN2	AIN2	LTD2260: Analog input 2 / IDAC1 / IDAC2 LTD2261: Analog input 2 / IDAC1 / IDAC2 / REFP1 / GPIO0 / $\overline{\text{ACX1}}$
31	AIN1	AIN1	Analog input 1 / IDAC1 / IDAC2 / REFN0
32	AIN0	AIN0	Analog input 0 / IDAC1 / IDAC2 / REFP0

9. Functional Block Diagram

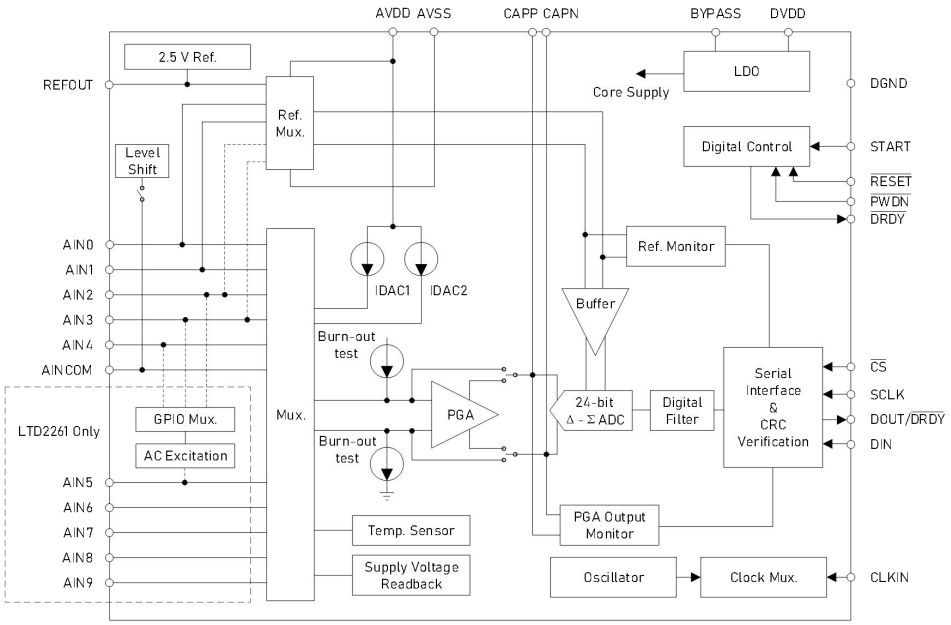

Figure X. Functional Block Diagram

10. Ordering Information

Part Number	Package Type	Quantity	Mark Code
LTD2260XF32/R10	QFN5×5-32L	Tape and Reel, 5000	D2260
LTD2261XF32/R10	QFN5×5-32L	Tape and Reel, 5000	D2261

11. Specifications

11.1. Limiting Value

Parameter	MIN	MAX	UNIT
AVDD to AVSS	-0.3	7	V
AVSS to DGND	-3	0.3	V
DVDD to DGND	-0.3	7	V
AINx	AVSS - 0.3	AVDD+0.3	V
SCLK, DIN, START, CLKIN, $\overline{CS}$, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, $\overline{RESET}$, $\overline{PWDN}$	DGND - 0.3	DVDD + 0.3	V
Continuous input current for all pins except for power supply pins	-10	10	mA
T_J		150	℃
T_{STG}	-60	150	℃

11.2. ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V

Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	V

11.3. Recommended Operating Conditions

Parameter		Conditions	Min	Nom	Max	Unit
Power Supply						
	Analog power supply	AVDD to AVSS	4.75	5	5.25	V
		AVSS to DGND	-2.6		0	V
	Digital power supply	DVDD to DGND	2.7		5.25	V
Analog Inputs						
V_{AINX}	Absolute input voltage	PGA mode	AVSS + 0.3 + V_{IN} × (Gain - 1) / 2		AVDD - 0.3 - V_{IN} × (Gain - 1) / 2	V
		PGA bypassed	AVSS - 0.1		AVDD + 0.1	
V_{IN}	Differential input voltage	V_{IN} = V_{AINP} - V_{AINN}		±V_{REF} / Gain		V
Voltage Reference Inputs						
V_{REF}	Differential reference voltage		0.9		AVDD-AVSS	V
V_{REFNX}	Negative reference voltage		AVSS - 0.05		V_{REFPX} - 0.9	V
V_{REFPX}	Positive reference voltage		V_{REFNX} + 0.9		AVDD + 0.05	V
External Clock						
f_{CLK}	Frequency	2.5 to 25.6 kSPS	1	7.3728	8	MHz
		40 kSPS	1	10.24	10.75	
	Duty cycle		40%		60%	
GPIOs						
	Input voltage		AVSS		AVDD	V
Digital Inputs						
	Input voltage		DGND		DVDD	V
Temperature						
T_A	Ambient temperature		-45		125	℃

11.4. Electrical Characteristics

Minimum and maximum specifications are measured from T_A = −40°C to +125°C; typical specifications are measured at T_A = 25°C; all specifications are measured at AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, PGA mode, gain = 1, and data rate = 20 SPS (unless otherwise noted).

Parameter		Conditions	Min	Typ	Max	Unit
Analog Inputs						
	Absolute input current	PGA mode, V_{AINX} = 2.5V		4		nA
		PGA bypass		200		
	Absolute input current drift			0.01		nA/℃
	Differential input current	PGA mode, V_{IN} = 19 mV		±0.1		nA
		PGA mode, V_{IN} = 2.5 V		±1		
		PGA mode, chop mode		±5		
		PGA bypass, V_{IN} = 2.5 V		±40		
	Differential input current drift			0.05		nA/℃
	Differential input impedance	PGA mode		1		GΩ
		PGA bypass		50		MΩ
	Crosstalk			0.1		µV/V
PGA						
	Gain option			1, 2, 4, 8, 16, 32, 64, 128		V/V
	Anti-alias filter frequency	$C_{CAPP, CAPN}$ = 4.7 nF		60		kHz
Performance						
	Resolution	No missing code	24			Bits

DR	Data rate		2.5		40,000	SPS
	Noise performance					
INL	Integral non-linearity	Gain = 1 to 16		±2		ppm_{FSR}
		Gain = 32 to 128		±3		
		Gain = 1 to 32 (40 kSPS)		±5		
V_{OS}	Offset voltage	TA = 25℃		±50 / Gain		µV
		TA = 25℃, chop mode		±0.2 / Gain		
		After calibration				
	Offset voltage drift	Gain = 1 to 8		100 / Gain		nV/℃
		Gain = 16 to 128		10		
		Chop mode, gain = 1 to 128		1		
	Offset voltage long-term drift	Gain = 1, 1000 hr		±0.1		µV
GE	Gain error	T_A = 25℃, gain = 1 to 128		±0.05%		
		After calibration				
	Gain drift	Gain = 1 to 128			4	ppm/℃
NMRR	Normal-mode 50 Hz and 60 Hz rejection ratio			See table X		
CMRR	Common-mode rejection ratio	DR = 20 SPS		130		dB
		DR = 400 SPS		115		
PSRR	Power-supply rejection ratio	AVSS and AVDD		100		dB
		DVDD		120		
Internal Oscillator						
f_{CLK}	Frequency	2.5 SPS to 25.6 kSPS		7.3728		MHz
		40 kSPS		10.24		
	Accuracy			±0.5%		
Voltage Reference Inputs						
	Absolute input current			±250		nA
	Input current vs voltage			15		nA/V
	Input current drift			0.2		nA/℃
	Input impedance			30		MΩ
Internal Voltage Reference						
	Output voltage			2.5		V
	Initial error	T_A = 25℃		±0.1%		
	Temperature drift	T_A = 0℃ to 85℃			9	ppm/℃
		T_A = -40℃ to 125℃			12	
	Long-term drift	1000 hr		±25		ppm
	Thermal hysteresis	First temperature cycle		±70		ppm
		Second temperature cycle		±20		
	Output current		-10		10	mA
	Load regulation			50		µV/mA
	Start-up time	Settling time to ±0.001% of the final value		100		ms
Excitation Current Sources （IDACs）						
	Output current options			50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000		µA
	Compliance range		AVSS		AVDD - 1.1	V
	Accuracy			±0.7%		
	Match error	Same current magnitudes		±0.1%		
		Different current magnitudes		±1%		
	Temperature drift	Absolute		50		ppm/℃
		Match drift, $I_{IDAC1} = I_{IDAC2}$			25	
Level-shift Voltage (VBIAS)						
	Voltage			(AVDD + AVSS) / 2		V
	Output impedance			100		Ω
Burn-out Current Sources						

	Current options	Sink and source		0.05, 0.2, 1, 10		µA
	Accuracy	0.05 µA range		0.05		µA
Temperature Sensor						
	Sensor voltage	T_A = 25℃				mV
	Temperature coefficient					µV/℃
Monitors						
	PGA output	Low		AVSS + 0.2		V
		High		AVDD - 0.2		
	Reference voltage	Low		0.4	0.6	V
GPIOs						
V_{OL}	Low-level output voltage	I_{OL} = -1 mA			0.2 × AVDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × AVDD			V
V_{IL}	Low-level input voltage				0.3 × AVDD	V
V_{IH}	High-level input voltage		0.7 × AVDD			V
	Input hysteresis			0.5		V
Digital Inputs / Outputs						
V_{OL}	Low-level output voltage	I_{OL} = -1 mA			0.2 × DVDD	V
		I_{OL} = -8 mA		0.2 × DVDD		
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × DVDD			V
		I_{OH} = 8 mA		0.75 × DVDD		
V_{IL}	Low-level input voltage				0.3 × DVDD	V
V_{IH}	High-level input voltage		0.7 × DVDD			V
	Input hysteresis			0.1		V
	Input leakage		-10		10	µA
Power Supply						
I_{AVDD}, I_{AVSS}	Analog supply current	PGA bypass		2.7		mA
		PGA mode, gain = 1 to 32		3.8		
		PGA mode, gain = 64 or 128		4.3		
		Power-down mode		2		µA
I_{AVDD}, I_{AVSS}	Analog supply current (by function)	Voltage reference		0.2		mA
		40 kSPS mode		0.5		
		Current sources		As user defined		
I_{DVDD}	Digital supply current	20 SPS		0.4		mA
		40 kSPS		0.6		
		Power-down mode		30		µA
PD	Power dissipation	PGA mode		20		mW
		Power-down mode		0.1		

11.5. Timing Requirements

Specified in full operating ambient temperature range, DVDD = 2.7 V to 5.25 V, pin DOUT/$\overline{DRDY}$ load: 20 pF || 100 kΩ to DGND.

Parameter		MIN	MAX	UNIT
Serial Interface				
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after CS falling edge	50		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	25		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	25		ns
$t_{c(SC)}$	SCLK period	97	10^6	ns
$t_{W(SCH)}$, $t_{W(SCL)}$	Pulse duration, SCLK high or low	40		ns
$t_{d(SCCS)}$	Delay time, last SCLK falling edge before $\overline{CS}$ rising edge	50		ns
$t_{W(CSH)}$	Pulse duration, $\overline{CS}$ high to reset interface	25		ns
$t_{d(SCIR)}$	Delay time, SCLK high or low to force interface auto-reset		65540	$1/f_{CLK}$
Reset				

$t_{W(RSTL)}$	Pulse duration, $\overline{RESET}$ low	4		$1/f_{CLK}$
Conversion Control				
$t_{W(STH)}$	Pulse duration, START high	4		$1/f_{CLK}$
$t_{w(STL)}$	Pulse duration, START low	4		$1/f_{CLK}$
$t_{su(DRST)}$	Setup time, START low or STOP command after $\overline{DRDY}$ low to stop next conversion (continuous mode)		100	$1/f_{CLK}$
$t_{h(DRSP)}$	Hold time, START low or STOP command after $\overline{DRDY}$ low to continue next conversion (continuous mode)	150		$1/f_{CLK}$

11.6. Switching Characteristics

Specified in full operating ambient temperature range, DVDD = 2.7 V to 5.25 V, pin DOUT/$\overline{DRDY}$ load: 20 pF || 100 kΩ to DGND.

Parameter		MIN	TYP	MAX	UNIT
Serial Interface					
$t_{W(DRH)}$	Pulse duration, $\overline{DRDY}$ high	16			$1/f_{CLK}$
$t_{P(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT/$\overline{DRDY}$ driven	0		50	ns
$t_{P(SCDO1)}$	Propagation delay time, SCLK rising edge to valid DOUT/$\overline{DRDY}$			40	ns
$t_{h(SCDO1)}$	Hold time, SCLK rising edge to invalid data on DOUT/$\overline{DRDY}$	0			ns
$t_{h(SCDO2)}$	Hold time, last SCLK falling edge of operation to invalid data on DOUT/$\overline{DRDY}$	15			ns
$t_{p(SCDO2)}$	Propagation delay time, last SCLK falling edge to valid data ready function on DOUT/$\overline{DRDY}$			110	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT/$\overline{DRDY}$ high impedance			50	ns
Reset					
$t_{p(RSCN)}$	Propagation delay time, $\overline{RESET}$ rising edge or RESET command to start of conversion	512			1/f
$t_{p(PRCM)}$	Propagation delay time, power-on threshold voltage to ADC communication		2^{16}		$1/f_{CLK}$
$t_{p(CMCN)}$	Propagation delay time, ADC communication to conversion start	512			$1/f_{CLK}$
AC Excitation					
$t_{d(ACX)}$	Delay time, phase-to-phase blanking period		8		$1/f_{CLK}$
$t_{c(ACX)}$	ACX period	2			t_{STDR}
Conversion Control					
$t_{p(STDR)}$	Propagation delay time, START high or START command to $\overline{DRDY}$ high			2	$1/f_{CLK}$