General Description

The LTC882x family of single-, dual-, and quad- channel amplifiers features a maximized ratio of gain bandwidth (GBW) to supply current and is ideal for battery-powered applications such as wearables, handsets, tablets, and portable medical devices. Featuring rail-to-rail input and output swings, a wide bandwidth of 500-kHz combined with ultra-low supply current (typical 6.6 µA at V_S=5.5V per amplifier) and low noise (6 $\mu V_{P\text{-}P}$ at 0.1 to 10 Hz) , the LTC882x family is an excellent choice for precision or general-purpose, low-current, low-voltage, battery-powered applications. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the LTC882x operational amplifiers provides ease-of-use to the circuit designer: integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection (5-kV HBM). The LTC882x amplifiers are optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V).

The LTC8821 (single) is available in both SOT23-5L and SC70-5L packages. The LTC8822 (dual) is offered in DFN-8L, SOIC-8L and MSOP-8L packages. The quad-channel LTC8824 is offered in both SOIC-14L and TSSOP-14L packages. All of the devices are specified over the extended temperature range of −40 ℃ to +125 ℃.

Features and Benefits

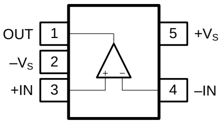
- 500 kHz GBW
- Ultra-Low 6.6 µA Supply Current (at 5.5V Supply, Per Amplifier)
- Low Input Offset Voltage: 0.5 mV
- Low Noise: 6 $\mu V_{P\text{-}P}$ at 0.1 to 10 Hz
- Single 1.8 V to 5.5 V Supply Voltage Range
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Extended Temperature Range: −40℃ to +125℃

Applications

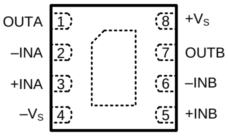
- Battery-Powered Instruments:
  - Consumer, Industrial, Medical, Notebooks
- Wearable Fitness Devices
- Audio Outputs
- Sensor Signal Conditioning:
  - Sensor Interfaces, Loop-Powered, Active Filters
- Wireless Sensors:
  - Home Security, Remote Sensing, Wireless Metering

Pin Configurations (Top View)

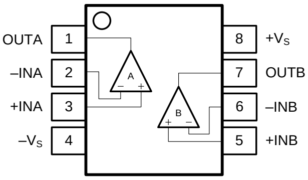
LTC8821
SOT23-5L / SC70-5L



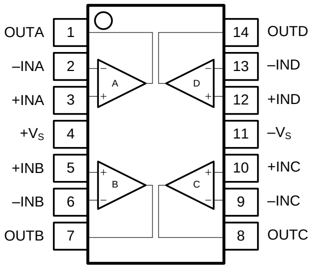
LTC8822
DFN-8L



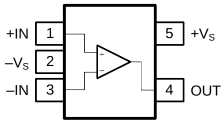
LTC8822
SOIC-8L / MSOP-8L



LTC8824
SOIC-14L / TSSOP-14L



LTC8823
SOT23-5L / SC70-5L



Pin Description

Symbol	Description
–IN	Inverting input of the amplifier.
+IN	Non-inverting input of the amplifier.
$+V_S$	Positive (highest) power supply.
$-V_S$	Negative (lowest) power supply.
OUT	Amplifier output.

Ordering Information

Type Number	Package Name	Package Quantity	Marking Code
LTC8821XT5/R6	SOT23-5	Tape and Reel, 3 000	AL1
LTC8821XC5/R6	SC70-5	Tape and Reel, 3 000	AL1
LTC8822XF8/R6	DFN2x2-8L	Tape and Reel, 3 000	AL2
LTC8822XF8S/R10	DFN1.5x1.5-8L	Tape and Reel, 5 000	AL2
LTC8822XS8/R8	SO-8	Tape and Reel, 4 000	AL2 X
LTC8822XV8/R6	MSOP-8	Tape and Reel, 3 000	AL2X
LTC8823XT5/R6	SOT23-5	Tape and Reel, 3 000	AL3
LTC8823XC5/R6	SC70-5	Tape and Reel, 3 000	AL3
LTC8824XS14/R5	SO-14	Tape and Reel, 2 500	AL4 X
LTC8824XT14/R6	TSSOP-14	Tape and Reel, 3 000	AL4 X

Limiting Value

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	10.0 V
Signal Input Terminals: Voltage, Current	V_{S-} – 0.3 V to V_{S+} + 0.3 V, ±10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	–65 ℃ to +150 ℃
Junction Temperature, T_J	150 ℃
Lead Temperature Range (Soldering 10 sec)	260 ℃

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9 (1)	±5 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014 (2)	±2 000	
	Machine model (MM), per JESD22-A115C	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

V_S = 5.0V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40 to +125 ℃.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±0.5	±2.5	mV
		T_A = −40 to +125 ℃			**±2.8**	
V_{OS} TC	Offset voltage drift	T_A = −40 to +125 ℃		**±0.5**	**±3**	µV/℃
PSRR	Power supply rejection ratio	V_S = 2.0 to 5.5 V, $V_{CM} < V_{S+}$ − 2V	98	115		dB
		T_A = −40 to +125 ℃	**88**			
INPUT BIAS CURRENT						
I_B	Input bias current			1		pA
		T_A = +85 ℃		150		
		T_A = +125 ℃		500		
I_{OS}	Input offset current			1		pA
NOISE						
V_n	Input voltage noise	f = 0.1 to 10 Hz		6		$µV_{P-P}$
e_n	Input voltage noise density	f = 10 kHz		62		nV/√Hz
		f = 1 kHz		63		
I_n	Input current noise density	f = 1 kHz		5		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		V_{S-}−0.1		V_{S+}+0.1	V
		T_A = −40 to +125 ℃	V_{S-}		V_{S+}−0.1	
CMRR	Common-mode rejection ratio	V_S = 5.5 V, V_{CM} = −0.1 to 5.5 V	76	92		dB
		V_{CM} = 0 to 5.3 V, T_A = −40 to +125 ℃	**70**			
		V_S = 2.0 V, V_{CM} = −0.1 to 2.0 V	72	86		
		V_{CM} = 0 to 1.8 V, T_A = −40 to +125 ℃	**68**			
INPUT IMPEDANCE						
R_{IN}	Input resistance		100			GΩ
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
A_{VOL}	Open-loop voltage gain	R_L = 25 kΩ, V_O = 0.05 to 3.5 V	86	97		dB
		T_A = −40 to +125 ℃	**80**			
		R_L = 5 kΩ, V_O = 0.15 to 3.5 V	80	92		
		T_A = −40 to +125 ℃	**74**			
FREQUENCY RESPONSE						
GBW	Gain bandwidth product			500		kHz
SR	Slew rate	G = +1, C_L = 100 pF, V_O = 1.5 to 3.5 V		0.25		V/µs
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, R_L = 2 kΩ, V_O = 1 V_{RMS}		0.005		%
t_S	Settling time	To 0.1%, G = +1, 1V step		6		µs
		To 0.01%, G = +1, 1V step		7		

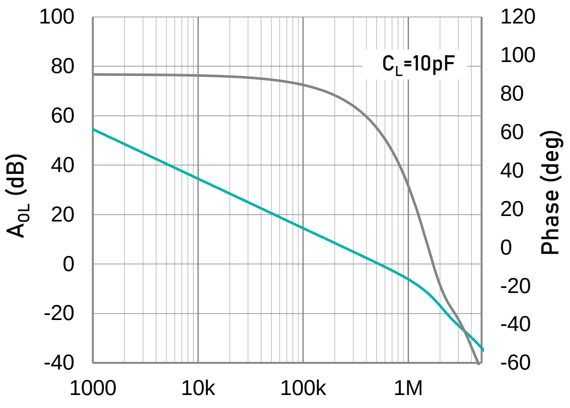
Electrical Characteristics (continued)

V_S = 5.0V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40 to +125 ℃.

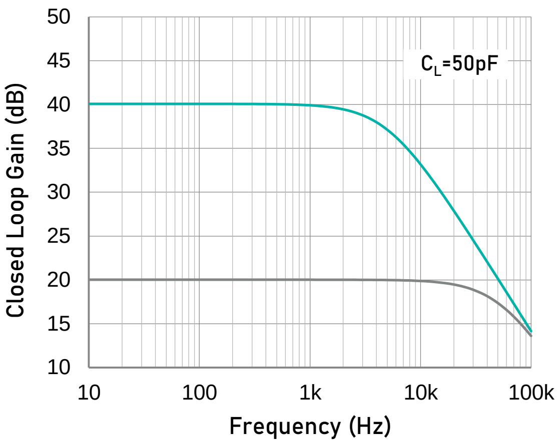
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{OR}	Overload recovery time	To 0.1%, V_{IN} * Gain > V_S		10		µs
OUTPUT						
V_{OH}	High output voltage swing	R_L = 25 kΩ	$V_{S+}-8$	$V_{S+}-5$		mV
		R_L = 5 kΩ	$V_{S+}-36$	$V_{S+}-26$		
V_{OL}	Low output voltage swing	R_L = 25 kΩ		$V_{S-}+4$	$V_{S-}+6$	mV
		R_L = 5 kΩ		$V_{S-}+16$	$V_{S-}+24$	
I_{SC}	Short-circuit current			±45		mA
POWER SUPPLY						
V_S	Operating supply voltage		1.8		5.5	V
I_Q	Quiescent current (per amplifier)	V_S = 2.0V, T_A = +25℃		5.2	6.5	µA
		V_S = 5.5V, T_A = +25℃		6.6	8.5	
		T_A = −40 to +125 ℃			**12**	
THERMAL CHARACTERISTICS						
T_A	Operating temperature range		-40		+125	℃
$θ_{JA}$	Package Thermal Resistance	SC70-5L		333		℃/W
		SOT23-5L		190		
		DFN2x2-8L		80		
		MSOP-8L		216		
		SOIC-8L		125		
		TSSOP-14L		112		
		SOIC-14L		115		

Typical Performance Characteristics

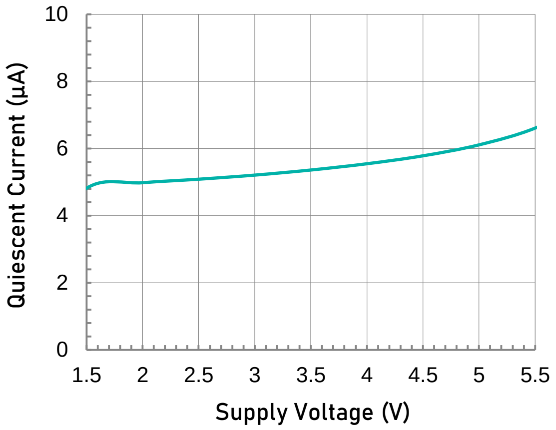
At T_A = +25℃, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.



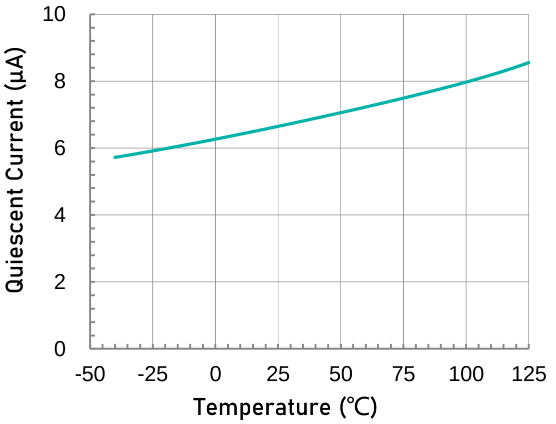
Open-loop Gain and Phase as a function of Frequency.



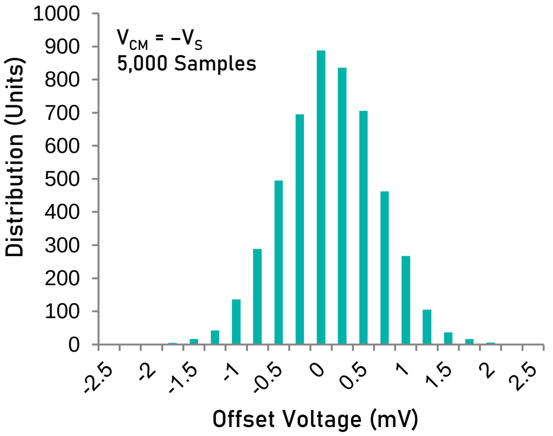
Closed-Loop Gain as a function of Frequency.



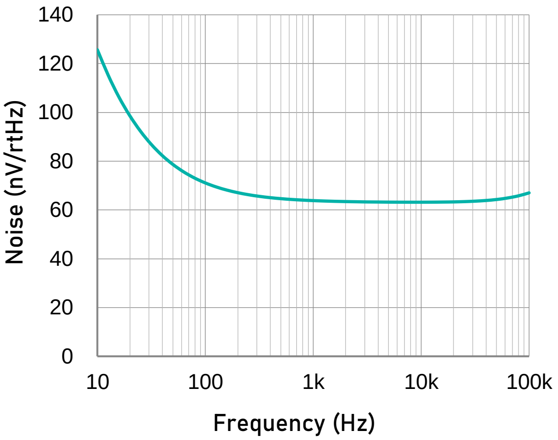
Quiescent Current as a function of Supply Voltage.



Quiescent Current as a function of Temperature.



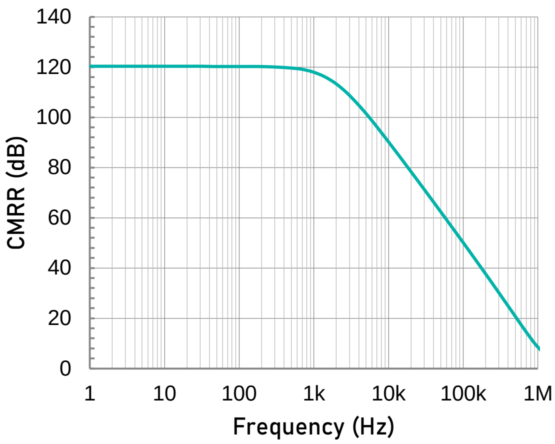
Offset Voltage Production Distribution



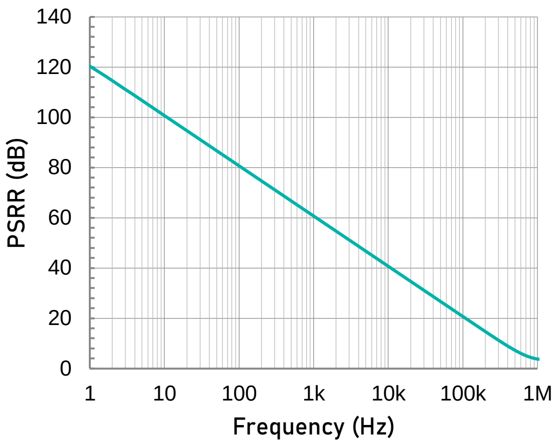
Input Voltage Noise Spectral Density as a function of Frequency.

Typical Performance Characteristics (continued)

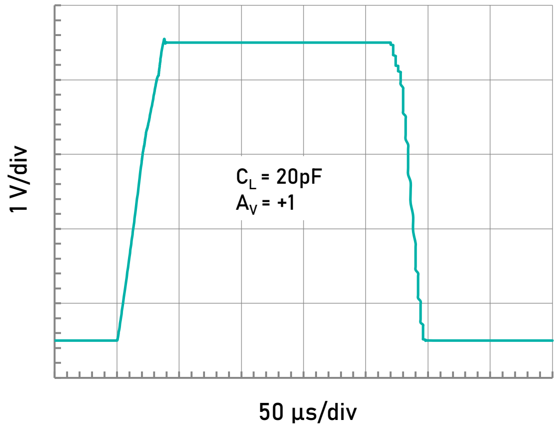
At T_A = +25℃, $V_{CM} = V_S/2$, and R_L = 10kΩ connected to $V_S/2$, unless otherwise noted.



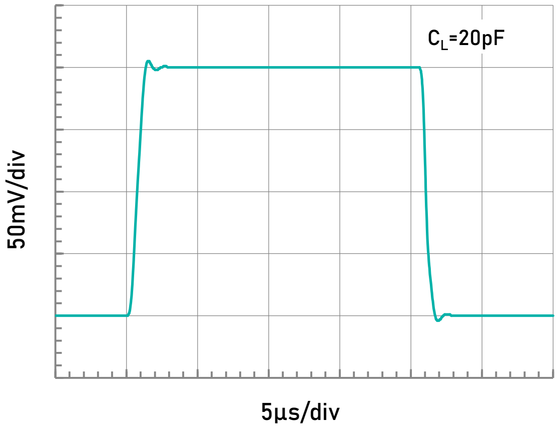
Common-mode Rejection Ratio as a function of Frequency.



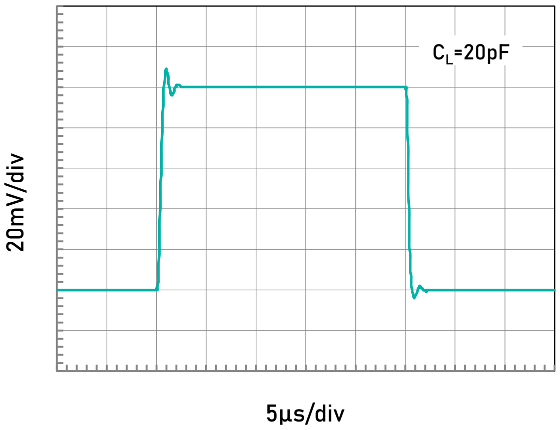
Power Supply Rejection Ratio as a function of Frequency.



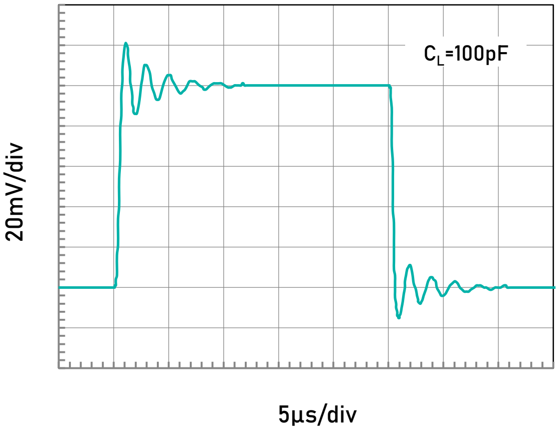
Large Signal Step Response (4V Step).



Small Signal Step Response (200mV Step).



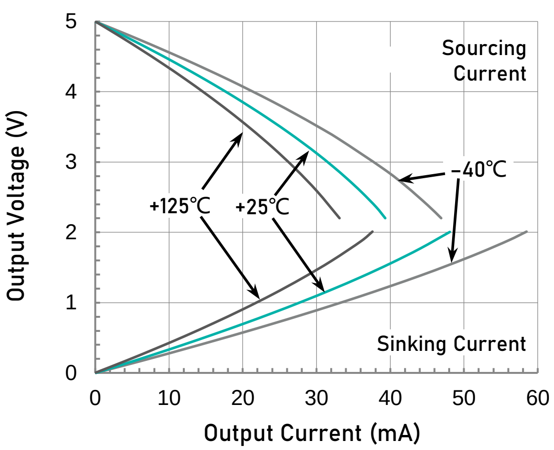
Small Signal Step Response (100mV Step).



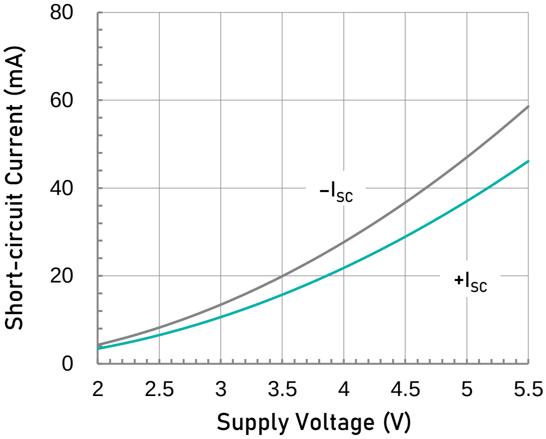
Small Signal Step Response (100mV Step).

Typical Performance Characteristics (continued)

At T_A = +25°C, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.



Output Voltage Swing as a function of Output Current.



Short-circuit Current as a function of Supply Voltage.

Application Notes

Featuring a maximized ratio of GBW-to-supply current, low operating supply voltage, low input bias current, and rail-to-rail inputs and outputs, the LTC882x family is an excellent choice for precision or general-purpose, low-current, low-voltage, battery-powered applications. These CMOS operational amplifiers consume an ultra-low 6.6-µA (typically at 5.5-V supply voltage) supply current per amplifier. The LTC882x family is unity-gain stable with a 500-kHz GBW product, driving capacitive loads up to 20-pF. The capacitive load can be increased to 500-pF when the amplifier is configured for a 5-V/V gain.

OPERATING VOLTAGE

The LTC882x family is optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V). In addition, many specifications apply from –40 ℃ to +125 ℃. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the LTC882x series extends 100-mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}–1.4 V to the positive supply, whereas the P-channel pair is active for inputs from 100-mV below the negative supply to approximately V_{S+}–1.4 V. There is a small transition region, typically V_{S+}–1.2 V to V_{S+}–1 V, in which both pairs are on. This 200-mV transition region can vary up to 200-mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}–1.4 V to V_{S+}–1.2 V on the low end, up to V_{S+}–1 V to V_{S+}–0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the LTC882x op-amps during normal operation is approximately 1-pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

INPUT EMI FILTER AND CLAMP CIRCUIT

Figure 1 shows the input EMI filter and clamp circuit. The LTC882x op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 300-mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA as stated in the Absolute Maximum Ratings.

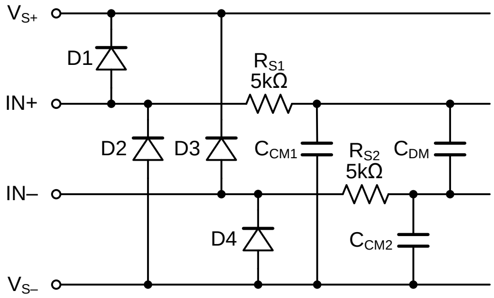


Figure 1. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the LTC882x family is composed of two 5-kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the −3 dB low-pass cutoff frequencies at 35-MHz for common-mode signals, and at 22-MHz for differential signals.

RAIL-TO-RAIL OUTPUT

Designed as a micro-power, low-noise operational amplifier, the LTC882x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 25-kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 5-kΩ, the output swings typically to within 26-mV of the positive supply rail and within 16-mV of the negative supply rail.

Application Notes (continued)

CAPACITIVE LOAD AND STABILITY

The LTC882x family of operational amplifiers is unity-gain stable for loads up to 20-pF. However, the capacitive load can be increased to 500-pF when the amplifier is configured for a minimum gain of 5-V/V.

As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to overshooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the LTC882x family requires greater capacitive-drive capability. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 2. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L. In unity gain applications with relatively small R_L (approximately 5-kΩ), the capacitive load can be increased up to 100-pF.

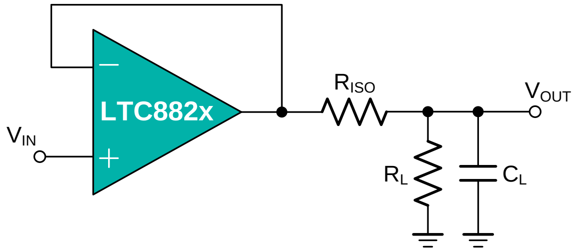


Figure 2. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 3. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

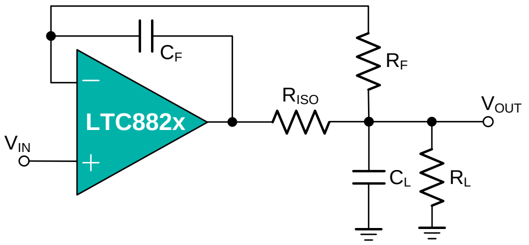


Figure 3. Indirectly Driving Heavy Capacitive Load with DC Accuracy

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

OVERLOAD RECOVERY

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the LTC882x family is approximately 10-µs.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The LTC882x op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN\_PEAK} / \Delta V_{OS})$$

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Application Notes (continued)

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the LTC882x op-amps, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 4 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

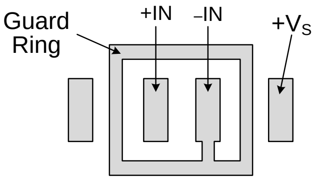


Figure 4. Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

Typical Application Circuits

DIFFERENTIAL AMPLIFIER

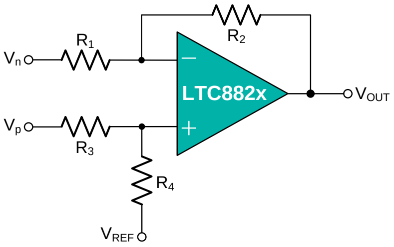
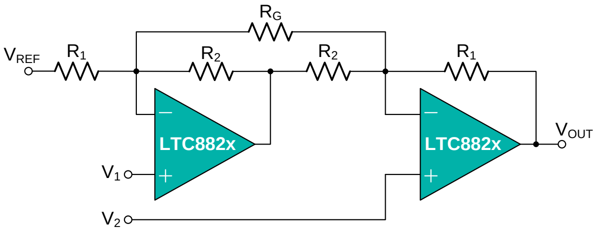


Figure 5. Differential Amplifier

The circuit shown in Figure 5 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then:

$$V_{OUT} = (V_p - V_n) \times R_2/R_1 + V_{REF}$$

INSTRUMENTATION AMPLIFIER



$$V_{OUT} = (V_1 - V_2)(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}) + V_{REF}$$

Figure 6. Instrumentation Amplifier

The LTC882x family is well suited for conditioning sensor signals in battery-powered applications. Figure 6 shows a two op-amp instrumentation amplifier, using the LTC882x op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, the V_{REF} is typically $V_S/2$.

BATTERY MONITORING

The low operating voltage and quiescent current of the LTC882x family make it an excellent choice for battery monitoring applications, as shown in Figure 7. In this circuit, V_{STATUS} is high as long as the battery voltage remains above 2-V (V_{REF} = 1.2V). A low-power reference is used to set the trip point. Resistor values are selected as follows:

1. R_F Selecting: Select R_F such that the current through R_F is approximately 1000x larger than the maximum bias current over temperature:
   $R_F = V_{REF} \div (1000 \times I_{BMAX}) = 1.2V \div (1000 \times 100pA) = 12M\Omega \approx 10M\Omega$
2. Choose the hysteresis voltage, V_{HYST}. For battery monitoring applications, 50-mV is adequate.
3. Calculate R_1 as follows:
   $R_1 = R_F \times (V_{HYST} \div V_{BATT}) \approx 10M\Omega \times (50mV \div 2.4V) = 210k\Omega$
4. Select a threshold voltage for V_{IN} rising (V_{TS}) = 2.0V.
5. Calculate R_2 as follows:
   $R_2 = 1 \div [V_{TS} \div (V_{REF} \times R_1) - 1 \div R_1 - 1 \div R_F] =$
   $1 \div [2V \div (1.2V \times 210k\Omega) - 1 \div 210k\Omega - 1 \div 10M\Omega]$
   $= 325k\Omega$
6. Calculate R_{BIAS}: The minimum supply voltage for this circuit is 1.8V. Providing 5µA of supply current assures proper operation. Therefore:
   $R_{BIAS} = (V_{BATTMIN} - V_{REF}) \div I_{BIAS} = (1.8V - 1.2V) \div 5\mu A = 120k\Omega$

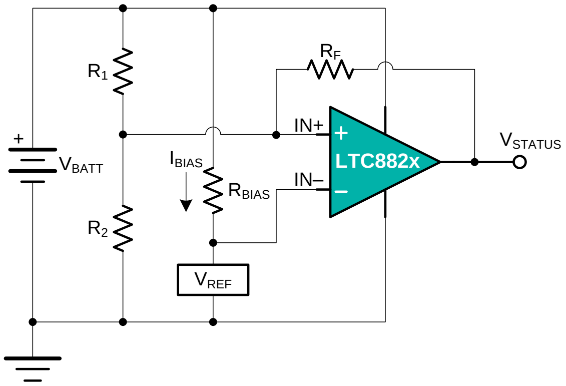


Figure 7. Battery Monitor

PORTABLE GAS METER

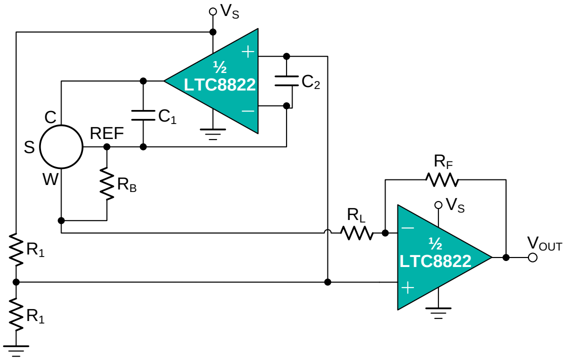
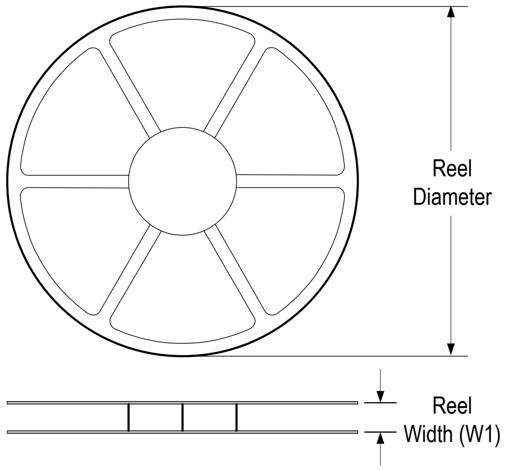


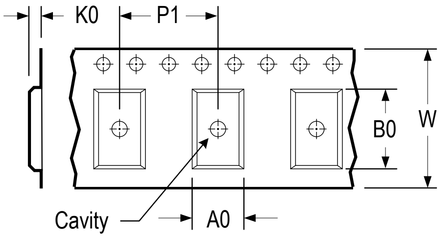
Figure 8. Portable Gas Meter Application

Tape and Reel Information

REEL DIMENSIONS

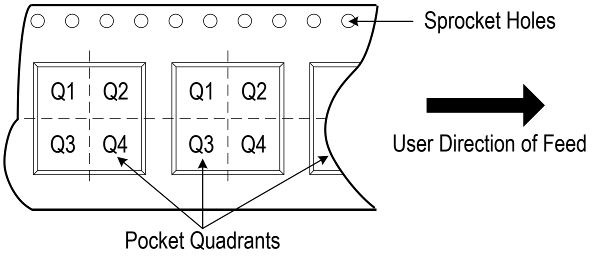


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

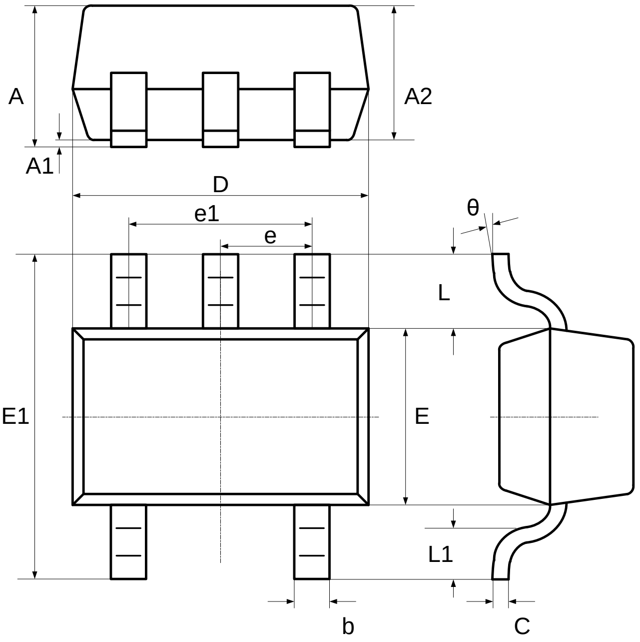


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTC8821XT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

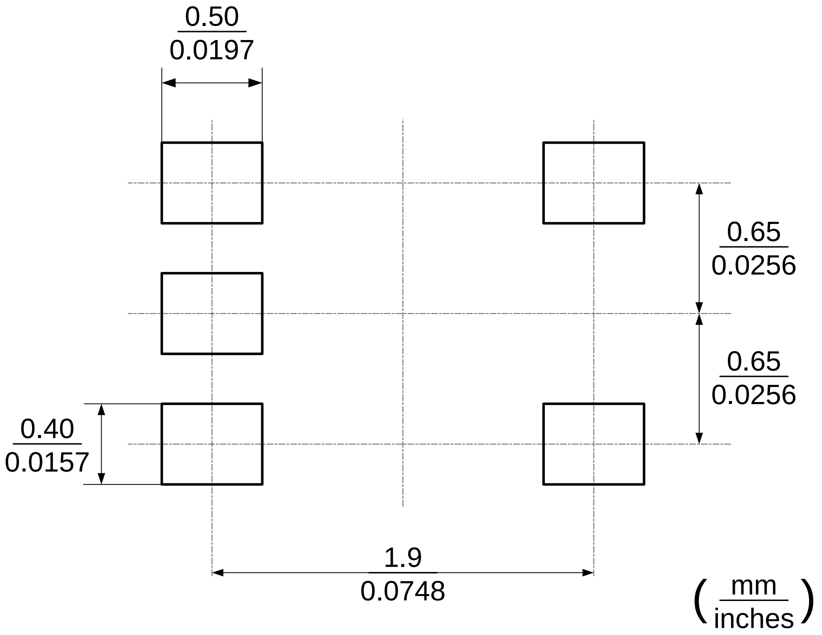
Package Outlines

DIMENSIONS, SC70-5L (SOT353)



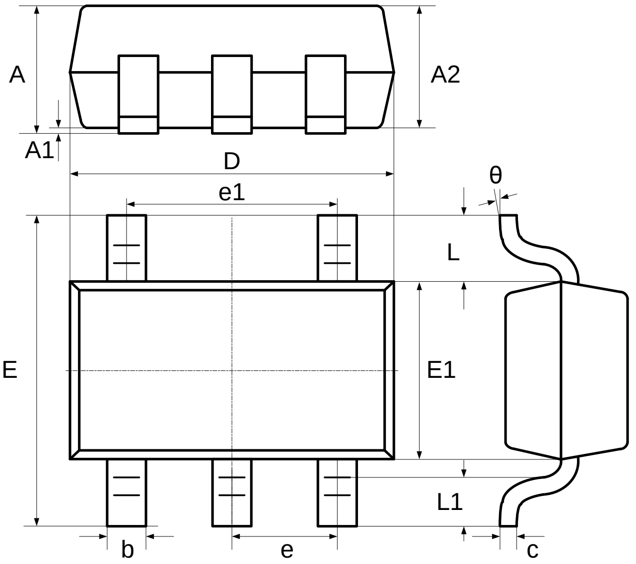
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.90	1.10	0.035	0.043
A1	0.00	0.10	0.000	0.004
A2	0.90	1.00	0.035	0.039
b	0.15	0.35	0.006	0.014
C	0.08	0.15	0.003	0.006
D	2.00	2.20	0.079	0.087
E	1.15	1.35	0.045	0.053
E1	2.15	2.45	0.085	0.096
e	0.65 typ.		0.026 typ.	
e1	1.20	1.40	0.047	0.055
L	0.525 ref.		0.021 ref.	
L1	0.26	0.46	0.010	0.018
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SC70-5L (SOT353)



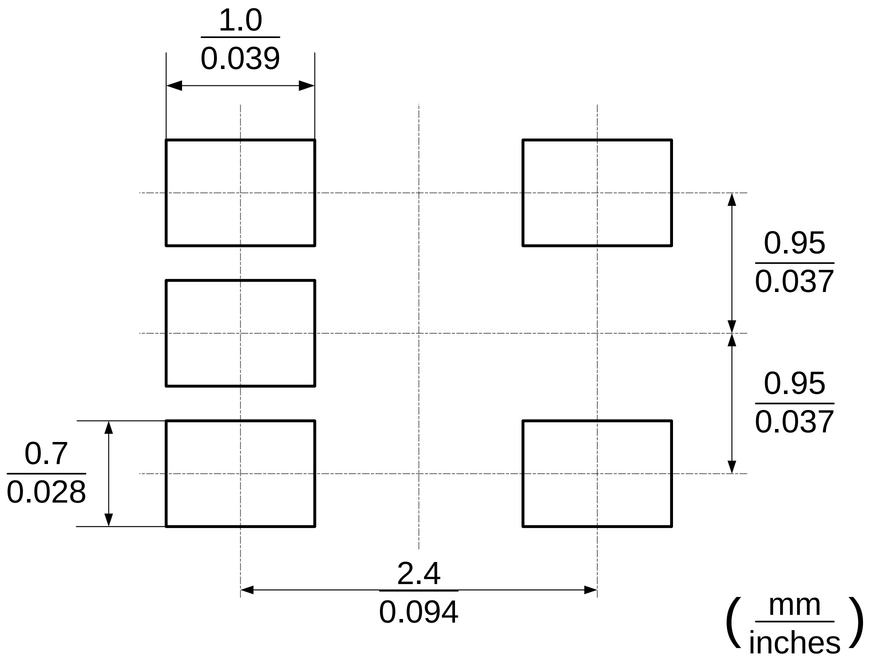
Package Outlines (continued)

DIMENSIONS, SOT23-5L



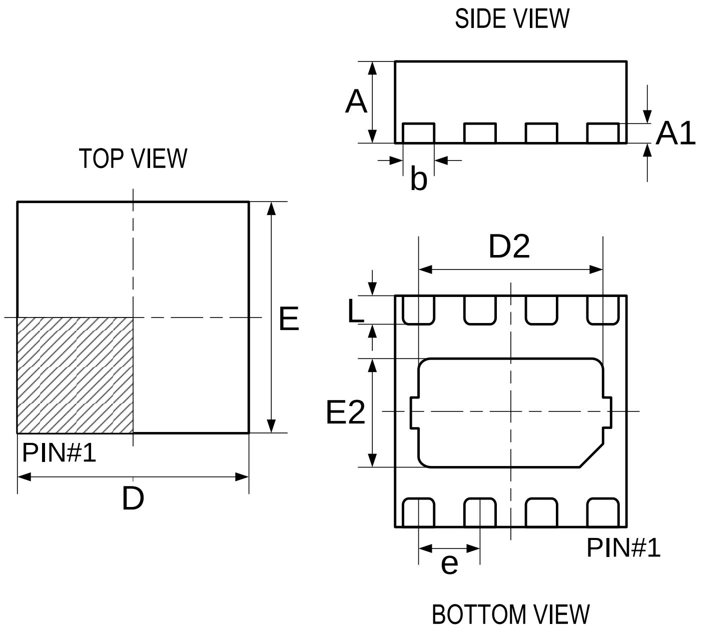
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.25	-	0.049
A1	0.04	0.10	0.002	0.004
A2	1.00	1.20	0.039	0.047
b	0.33	0.41	0.013	0.016
c	0.15	0.19	0.006	0.007
D	2.820	3.02	0.111	0.119
E1	1.50	1.70	0.059	0.067
E	2.60	3.00	0.102	0.118
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.60 REF		0.024 REF	
L1	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



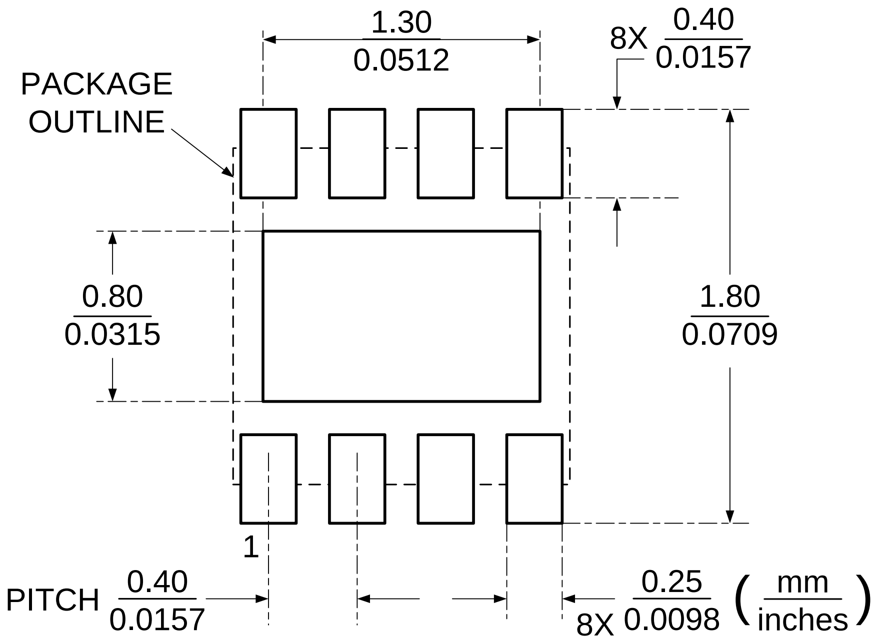
Package Outlines (continued)

DIMENSIONS, DFN1.5x1.5-8L



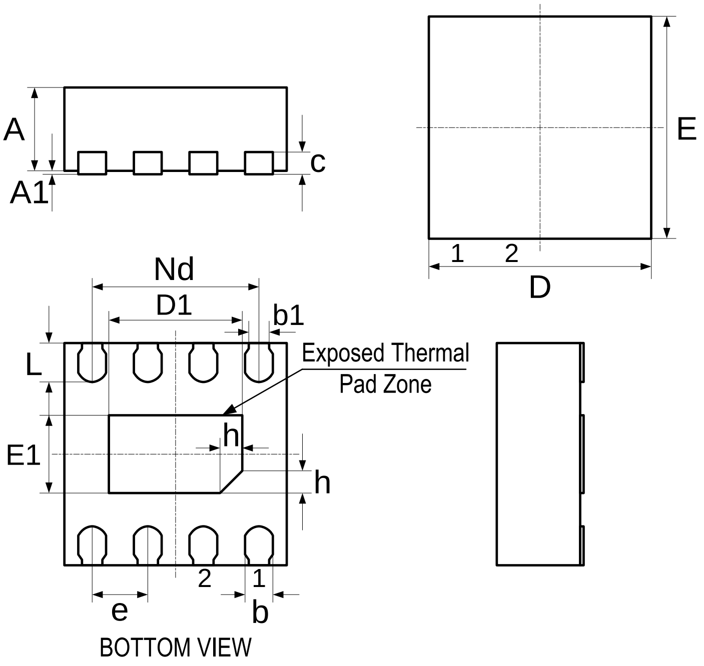
Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.48	0.53	0.58
A1	0.127 REF.		
b	0.15	0.20	0.25
D	1.45	1.50	1.55
D2	1.15	1.20	1.25
E	1.45	1.50	1.55
E2	0.65	0.70	0.75
e	0.40 BSC.		
L	0.125	0.175	0.225

RECOMMENDED SOLDERING FOOTPRINT, DFN1.5x1.5-8L



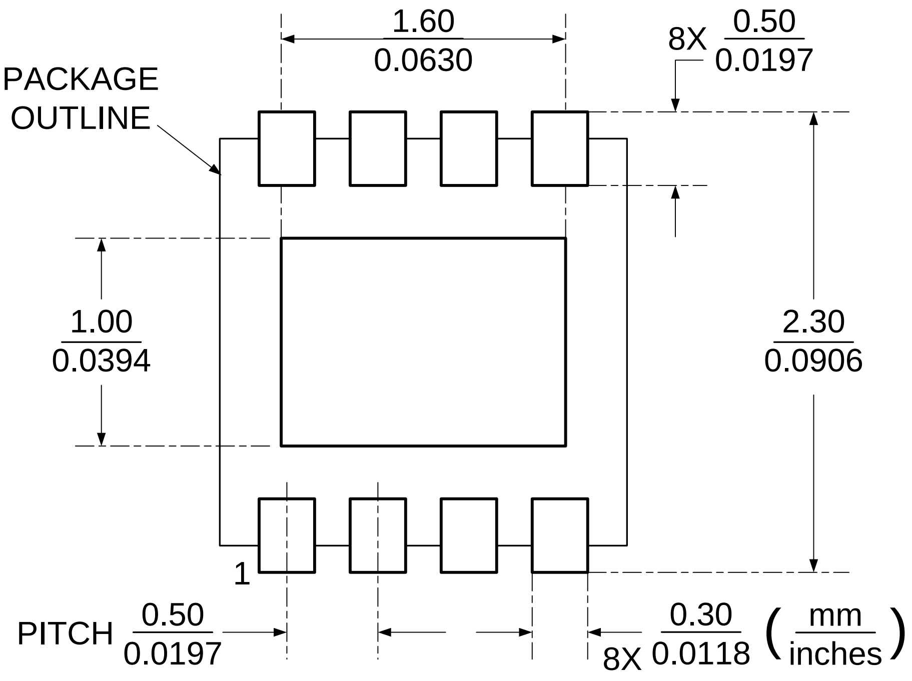
Package Outlines (continued)

DIMENSIONS, DFN2x2-8L



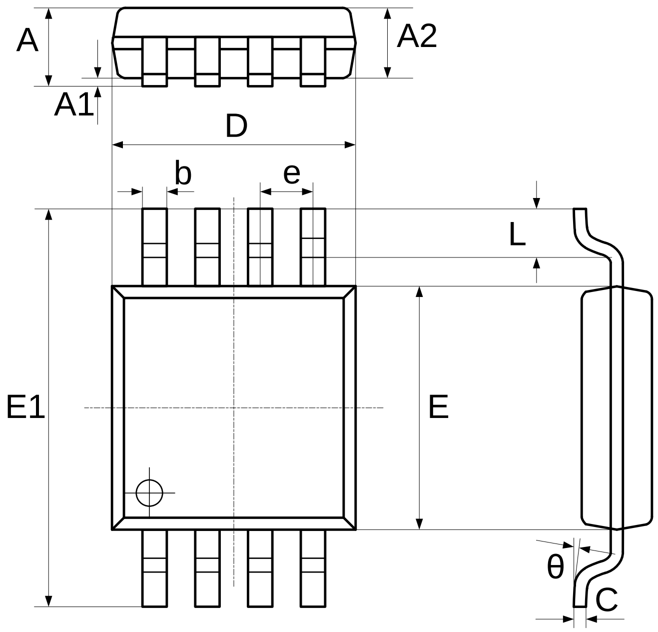
Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.20	0.25	0.30
b1	0.18 REF		
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D1	1.10	1.20	1.30
Nd	1.50BSC		
E	1.90	2.00	2.10
E1	0.60	0.70	0.80
e	0.50BSC		
L	0.30	0.35	0.40
h	0.15	0.20	0.25

RECOMMENDED SOLDERING FOOTPRINT, DFN2x2-8L



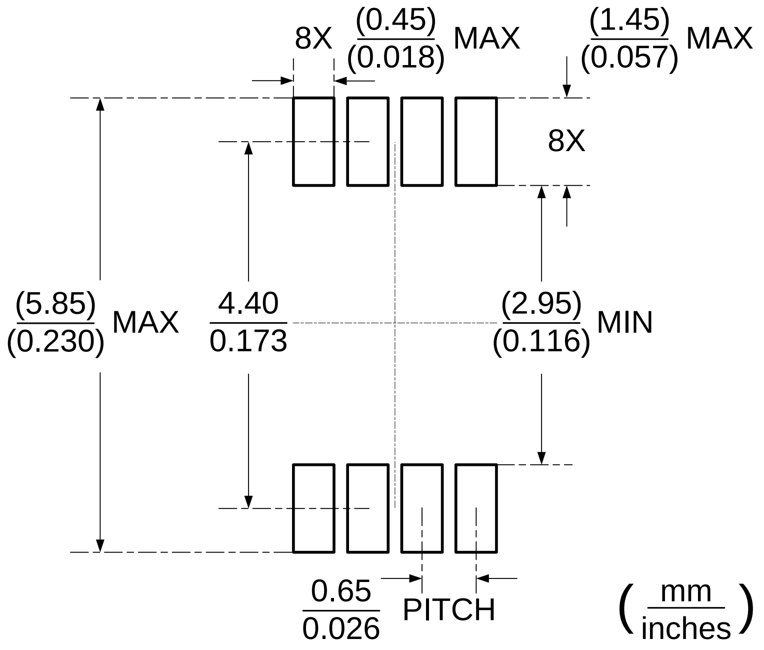
Package Outlines (continued)

DIMENSIONS, MSOP-8L



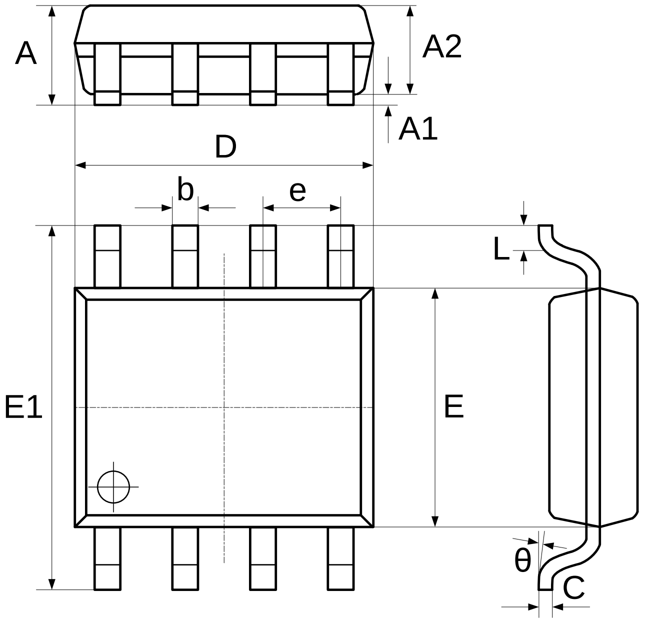
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.290	0.380	0.011	0.015
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650 TYP.		0.026 TYP.	
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



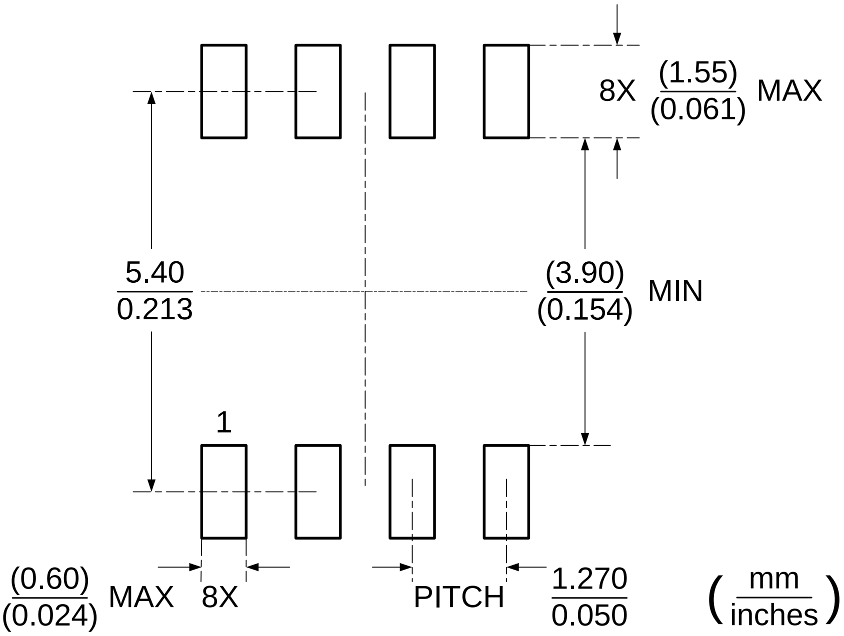
Package Outlines (continued)

DIMENSIONS, SOIC-8L



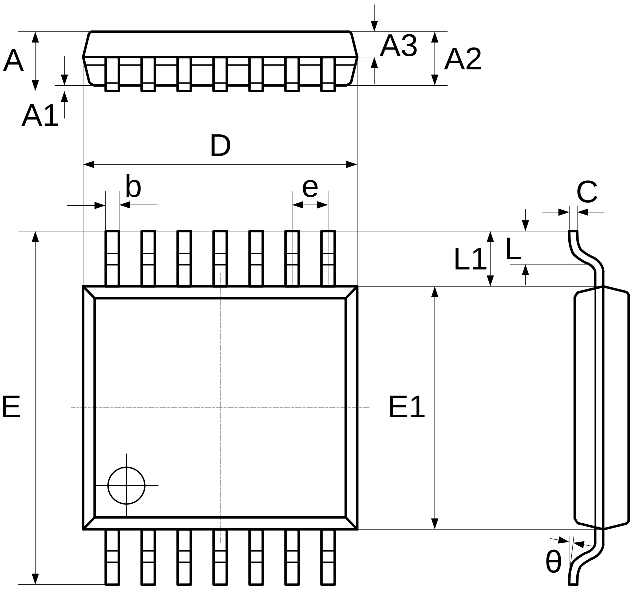
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.054	0.066
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.051	0.059
b	0.306	0.506	0.012	0.020
C	0.203 TYP.		0.008 TYP.	
D	4.700	5.100	0.185	0.201
E	3.820	4.020	0.150	0.158
E1	5.800	6.200	0.228	0.244
e	1.270 TYP.		0.050 TYP.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



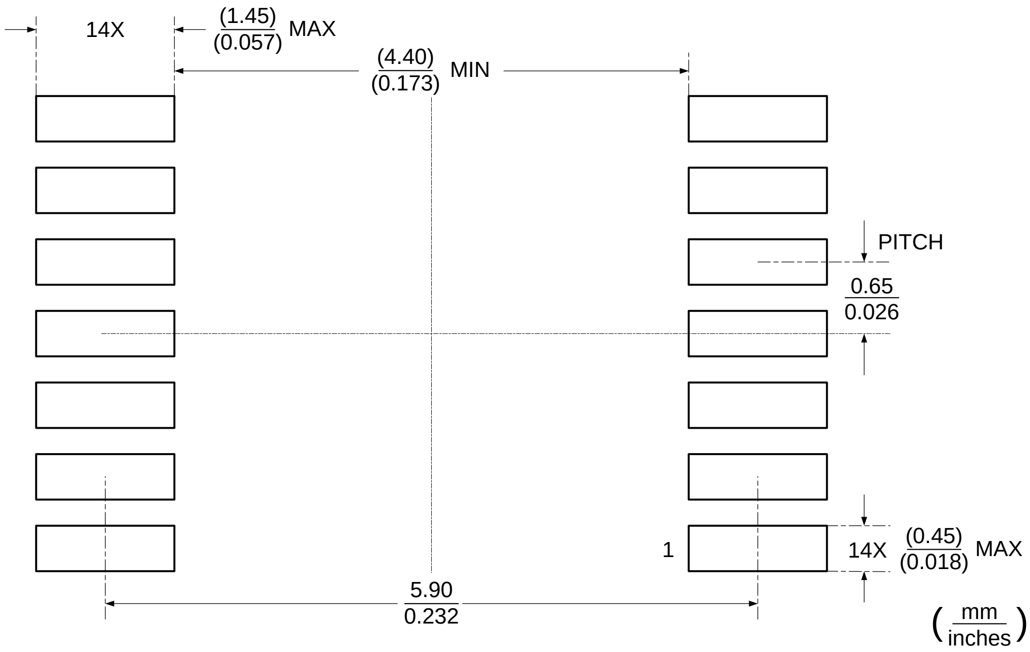
Package Outlines (continued)

DIMENSIONS, TSSOP-14L



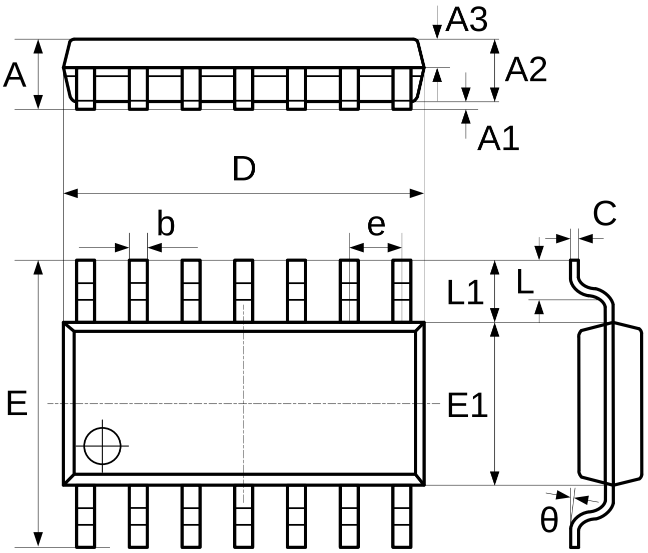
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
A3	0.390	0.490	0.015	0.019
b	0.200	0.290	0.008	0.011
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.191	0.199
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 TYP.		0.026 TYP.	
L1	1.000 REF.		0.039 REF.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L



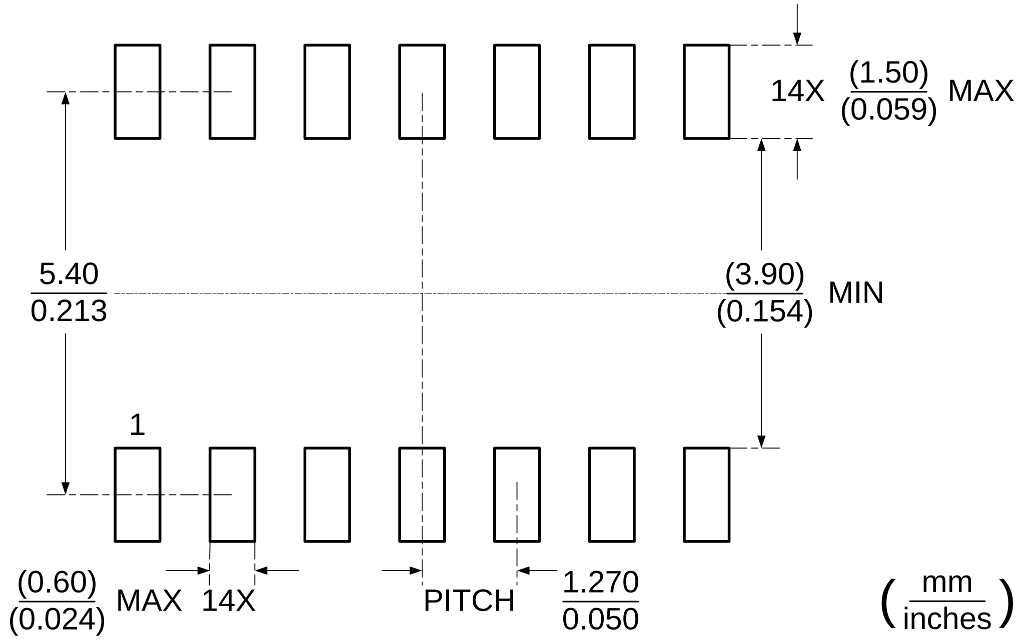
Package Outlines (continued)

DIMENSIONS, SOIC-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.057	0.073
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.053	0.061
A3	0.550	0.750	0.022	0.030
b	0.406 TYP.		0.016 TYP.	
C	0.203 TYP.		0.008 TYP.	
D	8.630	8.830	0.340	0.348
E	5.840	6.240	0.230	0.246
E1	3.850	4.050	0.152	0.159
e	1.270 TYP.		0.050 TYP.	
L1	1.040 REF.		0.041 REF.	
L	0.350	0.750	0.014	0.030
θ	2°	8°	2°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



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