General Description

The LTC8381/8382 of single- and dual- channel operational amplifiers provides input offset voltage correction for low offset (maximum ±50 µV) and drift (maximum 0.15 µV/°C) through the use of proprietary techniques. Featuring rail-to-rail input and output swings, and low quiescent current (typical 27 µA at 5 V supply) combined with a wide bandwidth of 350 kHz and very low noise (1.1 μV_{P-P} at 0.1 to 10 Hz) makes this family very attractive for a variety of battery-powered applications such as handsets, tablets, notebooks, and portable medical devices. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The LTC8381/8382 amplifiers are perfectly suited for applications that require precision amplification of low level signals, in which error sources cannot be tolerated, even in which high bandwidth and fast transition are needed. The rail-to-rail input and output swings make both high-side and low-side sensing easy. The LTC8381/8382 amplifiers can operate with a single supply voltage as low as 1.8V for 2-cell battery applications.

The LTC8381/8382 amplifers have enhanced EMI protection to minimize any electromagnetic interference from external sources, and have high electro-static discharge (ESD) protection (5-kV HBM). All models are specified over the extended industrial temperature range of −40°C to +125°C.

Features and Benefits

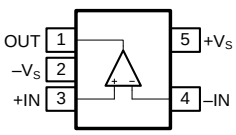
- DC Precision:
  - ±50 µV (maximum) V_{OS} with a Drift of ±0.15 µV/°C (maximum)
  - A_{V0L}: 106 dB (minimum)
  - PSRR: 103 dB (minimum)
  - CMRR: 92 dB (minimum,)
  - V_n: 1.1 μV_{PP} (typical, f = 0.1 to 10 Hz)
- 350 kHz Bandwidth and 0.2 V/µs Slew Rate
- Settling Time to 0.1% with 1V Step: 6 µs
- 27 µA Micropower and 1.8 V to 5.5 V Wide Supply Voltage Range
- Operating Temperature Range: −40°C to +125°C

Applications

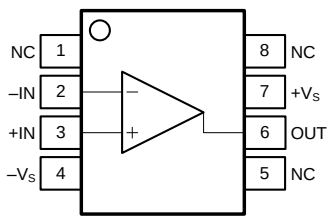
- Precision current sensing
- Battery-Powered Instruments:
  - Consumer, Industrial, Medical, Notebooks
- Resistor thermal detectors
- Temperature, position and pressure sensors
- Strain gage amplifiers
- Thermocouple amplifiers

Pin Configurations (Top View)

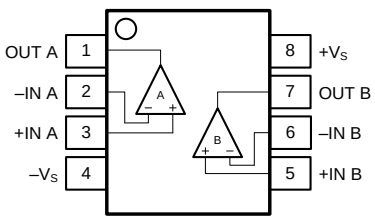
LTC8381
SOT23-5L



LTC8381
SOIC-8L



LTC8382
SOIC-8L / MSOP-8L



Pin Description

Symbol	Description
–IN	Inverting input of the amplifier.
+IN	Non-inverting input of the amplifier.
$+V_S$	Positive (highest) power supply.
$-V_S$	Negative (lowest) power supply.
OUT	Amplifier output.
NC	No internal connection.

Ordering Information

Orderable Type Number	Package Name	Package Quantity	Eco Class(1)	Operating Temperature	Marking Code
LTC8381XT5/R6	SOT23-5L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	–40℃ to +125℃	AC1
LTC8381XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	–40℃ to +125℃	AC1 X
LTC8382XV8/R6	MSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	–40℃ to +125℃	AC2X
LTC8382XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	–40℃ to +125℃	AC2 X

(1) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).
(2) Please contact to your Linearin representative for the latest availability information and product content details.

Limiting Value

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	10.0 V
Signal Input Terminals: Voltage, Current	V_{S-} – 0.3 V to V_{S+} + 0.3 V, ±10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	–65 ℃ to +150 ℃
Junction Temperature, T_J	150 ℃
Lead Temperature Range (Soldering 10 sec)	260 ℃

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9	±5 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014	±2 000	
	Machine model (MM), per JESD22-A115C	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

V_S = 5.0V, T_A = +25°C, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±10	±50	µV
V_{OS} TC	Offset voltage drift	T_A = −40 to +125 °C		**±0.02**	**±0.15**	µV/°C
PSRR	Power supply rejection ratio	V_S = 2.0 to 5.5 V, V_{CM} < V_{S+} − 2V	103	112		dB
		T_A = −40 to +125 °C	**96**			
INPUT BIAS CURRENT						
I_B	Input bias current			±70		pA
		T_A = +85 °C		±150		
		T_A = +125 °C		±800		
I_{OS}	Input offset current			±100		pA
NOISE						
V_n	Input voltage noise	f = 0.01 to 1 Hz		0.3		μV_{P-P}
		f = 0.1 to 10 Hz		1.1		
e_n	Input voltage noise density	f = 10 kHz		66		nV/√Hz
		f = 1 kHz		69		
I_n	Input current noise density	f = 1 kHz		0.1		pA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		V_{S-}−0.1		V_{S+}+0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, V_{CM} = −0.1 to 5.5 V	92	110		dB
		V_{CM} = 0 to 5.2 V, T_A = −40 to +125 °C	**86**			
		V_S = 2.0 V, V_{CM} = −0.1 to 2.0 V	85	106		
		V_{CM} = 0 to 1.7 V, T_A = −40 to +125 °C	**79**			
INPUT IMPEDANCE						
R_{IN}	Input resistance		100			GΩ
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
A_{VOL}	Open-loop voltage gain	R_L = 25 kΩ, V_O = 0.05 to 3.5 V	106	122		dB
		T_A = −40 to +125 °C	**100**			
		R_L = 5 kΩ, V_O = 0.15 to 3.5 V	102	114		
		T_A = −40 to +125 °C	**96**			
FREQUENCY RESPONSE						
GBW	Gain bandwidth product	f = 1 kHz		350		kHz
SR	Slew rate	G = +1, C_L = 100 pF, V_O = 1.5 to 3.5 V		0.2		V/µs
t_S	Settling time	To 0.1%, G = +1, 1V step		6		µs
		To 0.01%, G = +1, 1V step		7		
t_{OR}	Overload recovery time	To 0.1%, V_{IN} * Gain > V_S		55		µs

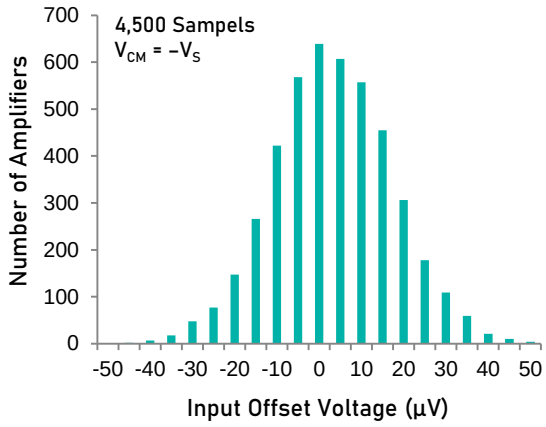
Electrical Characteristics (continued)

V_S = 5.0V, T_A = +25°C, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

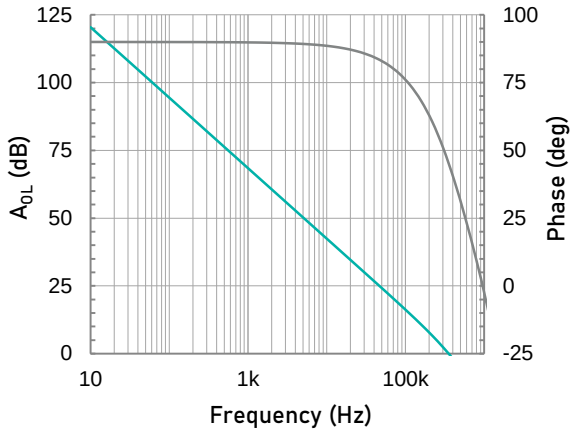
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OUTPUT						
V_{OH}	High output voltage swing	R_L = 25 kΩ	V_{S+}−10	V_{S+}−5		mV
		R_L = 5 kΩ	V_{S+}−40	V_{S+}−25		
V_{OL}	Low output voltage swing	R_L = 25 kΩ		V_{S-}+4	V_{S-}+8	mV
		R_L = 5 kΩ		V_{S-}+16	V_{S-}+30	
Z_{OUT}	Open-loop output impedance	f = 20 kHz, I_O = 0		2		kΩ
I_{SC}	Short-circuit current	Source current through 10Ω		40		mA
		Sink current through 10Ω		50		
POWER SUPPLY						
V_S	Operating supply voltage	T_A = −40 to +125 °C	1.8		5.5	V
I_Q	Quiescent current (per amplifier)			27	40	µA
THERMAL CHARACTERISTICS						
T_A	Operating temperature range		-40		+125	°C
$θ_{JA}$	Package Thermal Resistance	SOT23-5L		190		°C/W
		MSOP-8L		216		
		SOIC-8L		125		

Typical Performance Characteristics

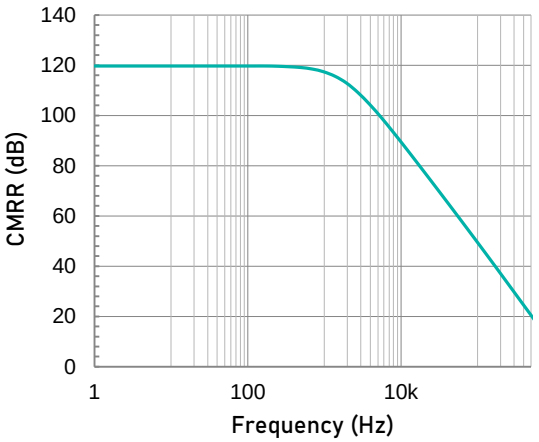
At T_A=+25°C, V_S=±2.5V, V_{CM}=V_S/2, R_L=10kΩ connected to V_S/2, and C_L=100pF, unless otherwise noted.



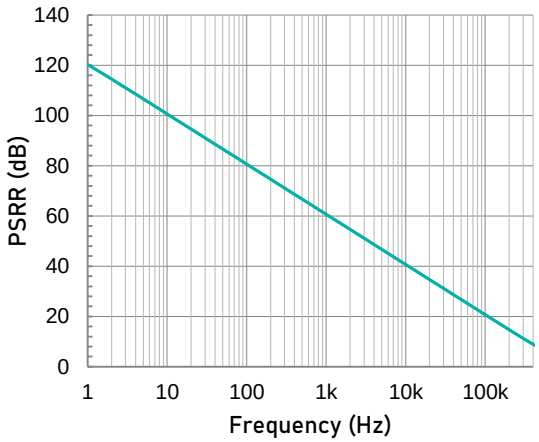
Input Offset Voltage Production Distribution.



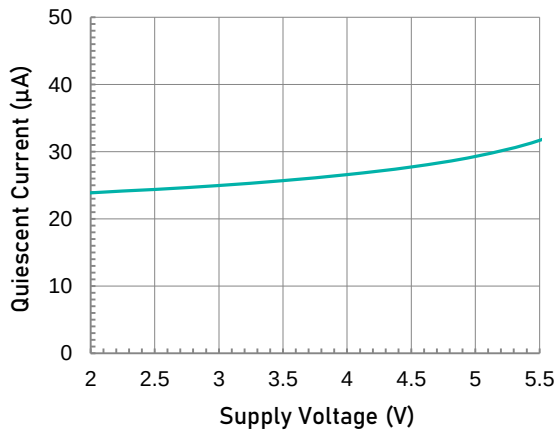
Open-loop Gain and Phase as a function of Frequency.



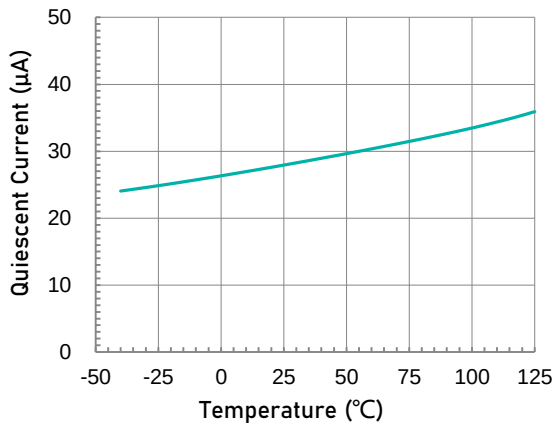
Common-mode Rejection Ratio as a function of Frequency.



Power Supply Rejection Ratio as a function of Frequency.



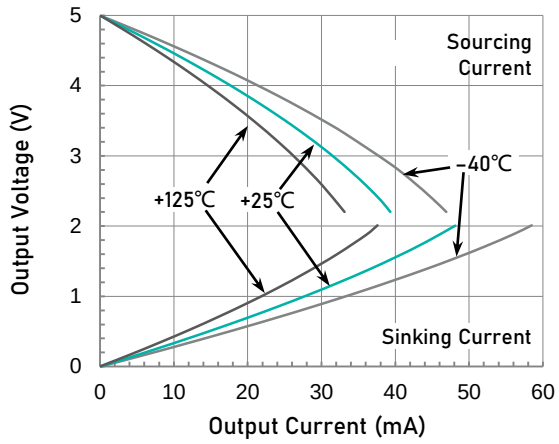
Quiescent Current as a function of Supply Voltage.



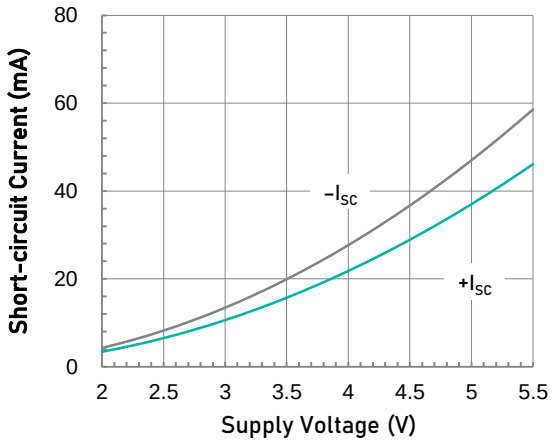
Quiescent Current as a function of Temperature.

Typical Performance Characteristics (continued)

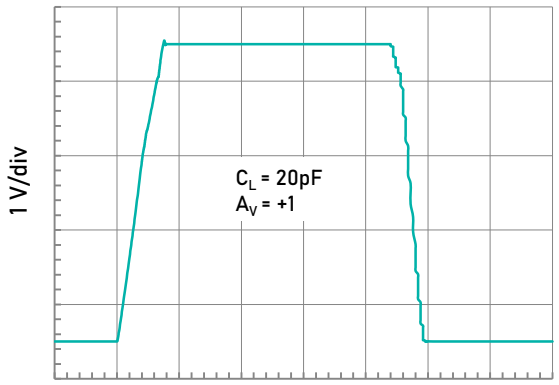
At T_A = +25°C, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.



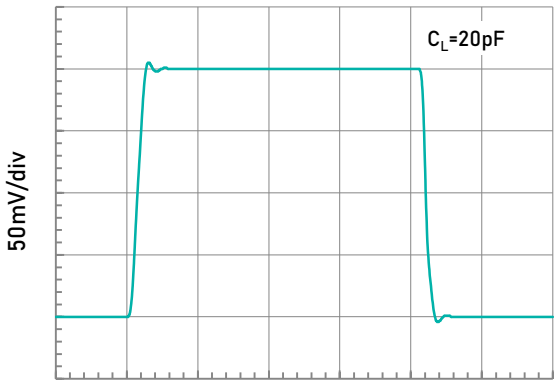
Output Voltage Swing as a function of Output Current.



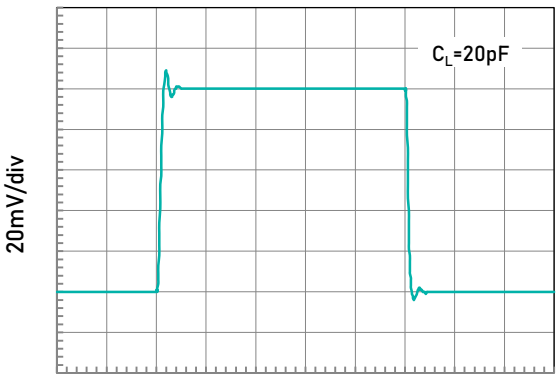
Short-circuit Current as a function of Supply Voltage.



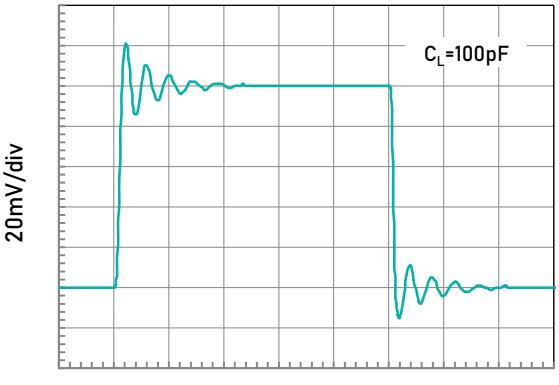
Large Signal Step Response (4V Step).



Small Signal Step Response (200mV Step).



Small Signal Step Response (100mV Step).



Small Signal Step Response (100mV Step).

Application Notes

The LTC8381/8382 operational amplifiers are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1µV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The LTC8381/8382 amplifier is fully specified and ensured for operation from 1.8V to 5.5V (±0.9V to ±2.75V). In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

NOTE: Supply voltages (V_{S+} to V_{S-}) higher than +10V can permanently damage the device.

INPUT VOLTAGE

The input common-mode voltage range of the LTC8381/8382 amplifier extends 100mV beyond the negative supply rail and reaches the positive supply rail. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}–1.4V to the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately V_{S+}–1.4V. There is a small transition region, typically V_{S+}–1.2V to V_{S+}–1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}–1.4V to V_{S+}–1.2V on the low end, up to V_{S+}–1V to V_{S+}–0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the LTC8381/8382 during normal operation is approximately 50pA. In over-driven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

INPUT EMI FILTER AND CLAMP CIRCUIT

Figure 1 shows the input EMI filter and clamp circuit. The LTC8381/8382 have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 300mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See the table of Absolute Maximum Ratings for more information.

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the LTC8381/8382 amplifier is composed of two 5-kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the –3dB low-pass cutoff frequencies at 35-MHz for common-mode signals, and at 22-MHz for differential signals.

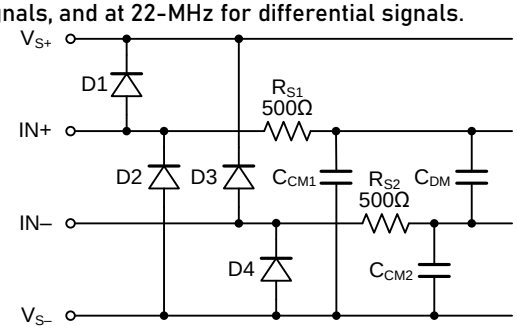


Figure 1. Input EMI Filter and Clamp Circuit

Application Notes (continued)

CAPACITIVE LOAD AND STABILITY

The LTC8381/8382 operational amplifiers can safely drive capacitive loads of up to 500pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the LTC8381/8382 must drive a load exceeding 500pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 2. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

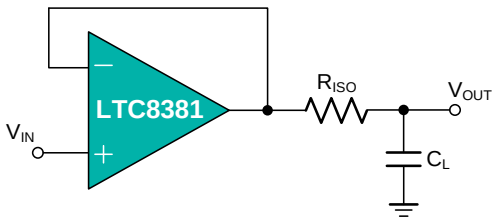


Figure 2. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 3. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

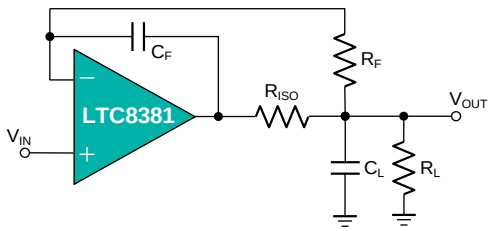


Figure 3. Indirectly Driving Heavy Capacitive Load with DC Accuracy

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

OVERLOAD RECOVERY

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the LTC8381/8382 amplifiers is approximately 55µs.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The LTC8381/8382 op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN\_PEAK} / \Delta V_{OS})$$

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the LTC8381/8382, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and

Application Notes (continued)

provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 4 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

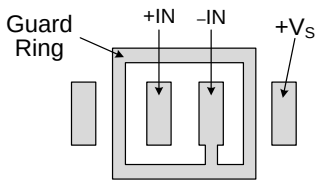


Figure 4. Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Typical Application Circuits

PRECISION LOW-SIDE CURRENT SHUNT SENSING

Many applications require the sensing of signals near the positive or negative rails. Current shunt sensing is one such application and is mostly used for feedback control systems. It is also used in a variety of other applications, including power metering, battery fuel gauging, and feedback controls in industrial applications. In such applications, it is desirable to use a shunt with very low resistance to minimize series voltage drop. This configuration not only minimizes wasted power, but also allows the measurement of high currents while saving power.

A typical shunt may be 100mΩ. At a measured current of 1A, the voltage produced from the shunt is 100mV, and the amplifier error sources are not critical. However, at low measured current in the 1mA range, the 100µV generated across the shunt demands a very low offset voltage and drift amplifier to maintain absolute accuracy.

The unique attributes of a zero drift amplifier provide a solution. Figure 5 shows a low-side current sensing circuit using the LTC8381/8382. The LTC8381/8382 op-amps are configured as difference amplifiers with a gain of 1000. Although the LTC8381/8382 op-amps have high CMRR, the CMRR of the system is limited by the external resistors. Therefore, the key to high CMRR for the system is resistors that are well matched from both the resistive ratio and relative drift, where $R_1/R_2 = R_3/R_4$. The transfer function is given by:

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} = (R_{SHUNT} \times I_{LOAD}) \times (R_2 / R_1) = 100 \times I_{LOAD}$$

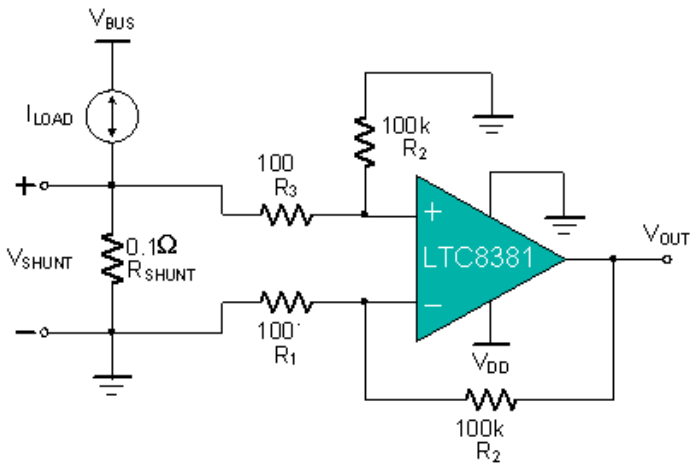


Figure 5. Low-Side Current Sensing Circuit

Any unused channel of the LTC8381/8382 must be configured in unity gain with the input common-mode voltage tied to the midpoint of the power supplies.

BIDIRECTIONAL CURRENT-SENSING

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1A to +1A. The single-ended output spans from 110mV to 3.19V. This design uses the LTC8381/8382 because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 6 shows the solution. This solution has the following requirements:

- Supply voltage: 3.3V
- Input: –1A to +1A
- Output: 1.65V±1.54V (110mV to 3.19V)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

Typical Application Circuits

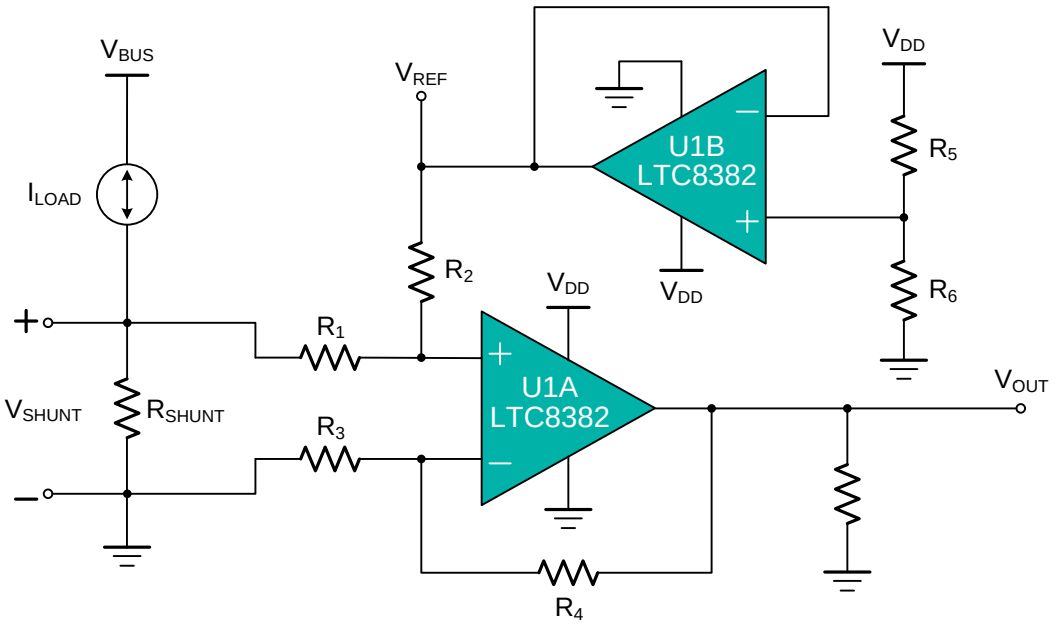


Figure 6. Bidirectional Current-Sensing Schematic

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1 and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U2. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF}$$

Where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = R_4 / R_3$
- $V_{REF} = V_{DD} \times [R_6 / (R_5 + R_6)]$ (1)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100mV and maximum load current of 1A.

$$R_{SHUNT(MAX)} = V_{SHUNT(MAX)} / I_{LOAD(MAX)} = 100mV / 1A = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100mV to +100mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1. Take care to ensure that the voltage present at the non-inverting node of U1 is within the common-mode range of the device. Therefore, use an operational amplifier, such as the LTC8381/8382, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the LTC8381/8382 has a maximum offset voltage of merely ±50 µV.

Given a symmetric load current of –1A to +1A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10kΩ resistors were used.

Typical Application Circuits

To set the gain of the difference amplifier, the common-mode range and output swing of the LTC8381/8382 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the LTC8381/8382 given a 3.3V supply.

- $-100mV < V_{CM} < 3.4V$ (3)
- $100mV < V_{OUT} < 3.2V$ (4)

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$Gain_{Diff\_Amp} = (V_{OUT\_MAX} - V_{OUT\_MIN}) / [R_{SHUNT} \times (I_{MAX} - I_{MIN})]$$
$$= (3.2V - 100mV) / 100m\Omega \times [1A - (-1A)] = 15.5\ V/V \quad (5)$$

The resistor value selected for R_1 and R_3 was 1kΩ. 15.4kΩ was selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

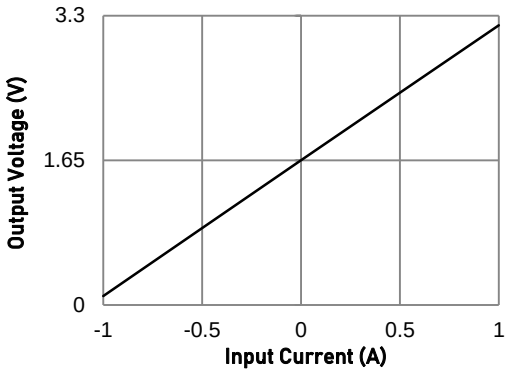


Figure 7. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs. Input Current

HIGH-SIDE VOLTAGE-TO-CURRENT (V-I) CONVERTER

The circuit shown in Figure 8 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0V to 2V to and output current of 0mA to 100mA.

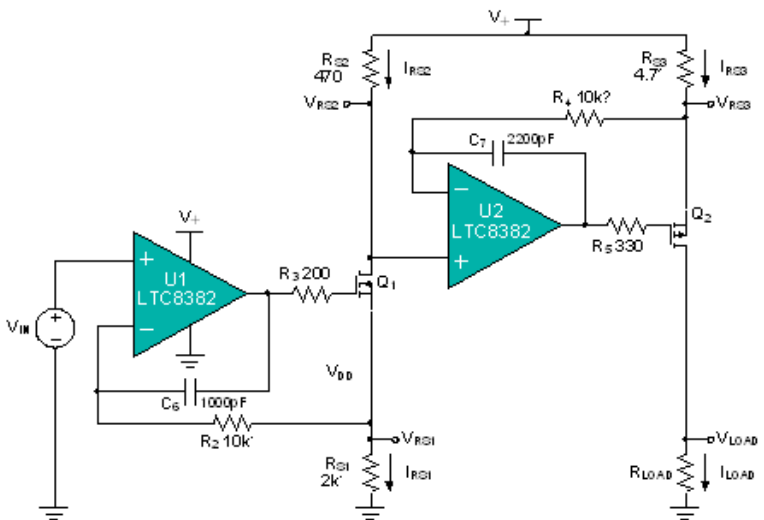


Figure 8. Bidirectional Current-Sensing Schematic

Typical Application Circuits

The design requirements are as follows:

- Supply Voltage: 5V DC
- Input: 0V to 2V DC
- Output: 0mA to 100mA DC

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The LTC8381/8382 CMOS operational amplifier is a high-precision, maximum ±50µV offset, maximum 0.15µV/℃ drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 5mV (at R_L = 25kΩ) of the positive rail. The LTC8381/8382 uses proprietary techniques to provide low initial offset voltage and very low drift over temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the LTC8381/8382 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

Figure 9 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the LTC8381/8382 facilitate excellent dc accuracy for the circuit.

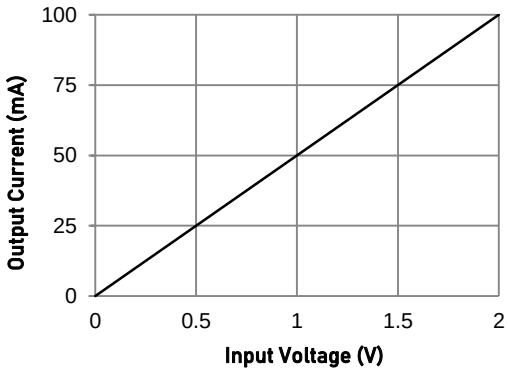
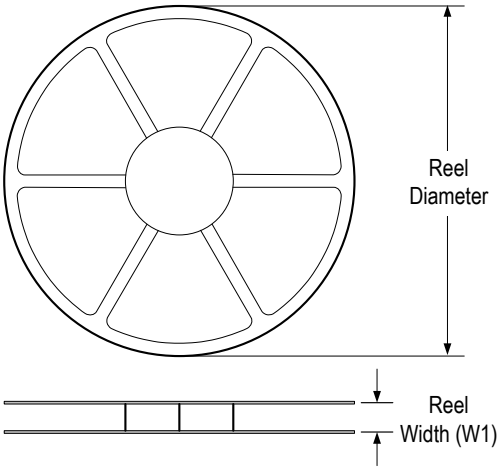


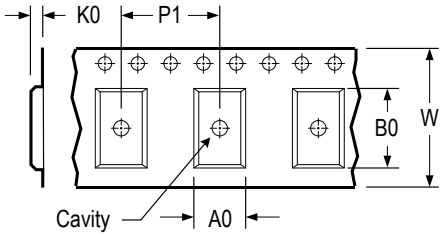
Figure 9. Measured Transfer Function for High-Side V-I Converter

Tape and Reel Information

REEL DIMENSIONS

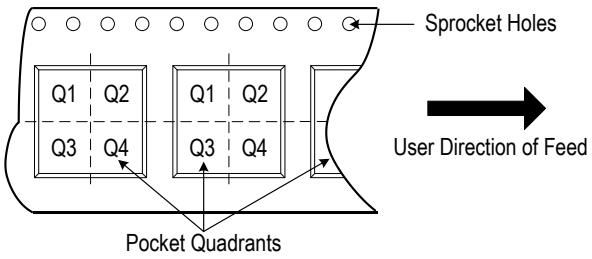


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

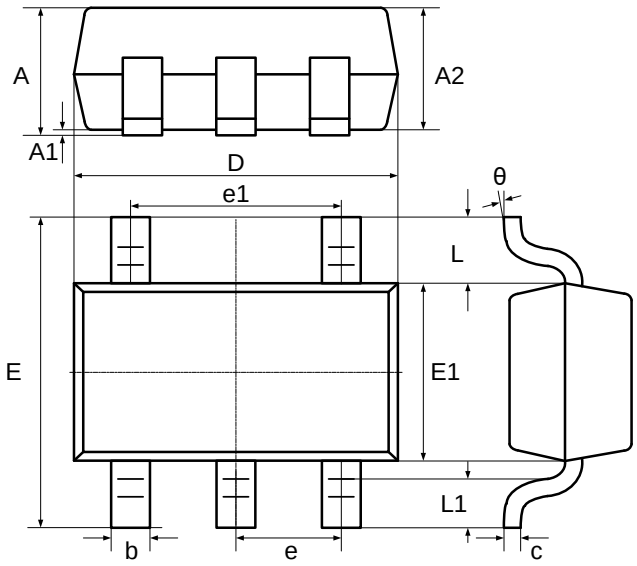


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTC8381XT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

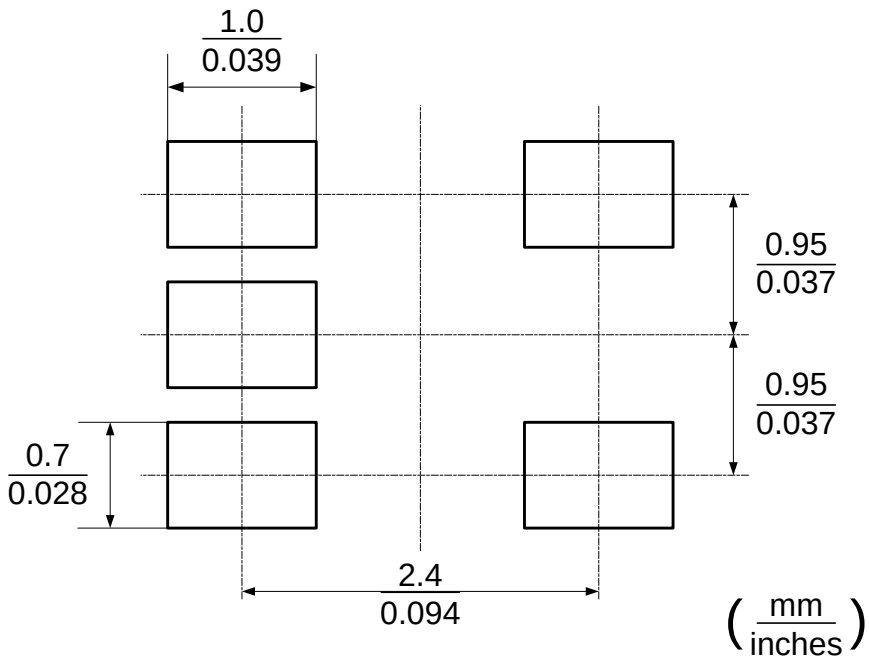
Package Outlines

DIMENSIONS, SOT23-5L



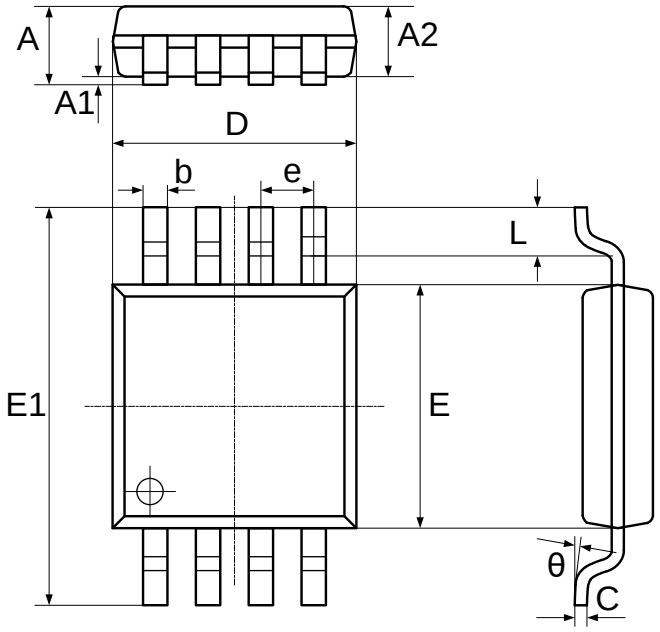
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.25	-	0.049
A1	0.04	0.10	0.002	0.004
A2	1.00	1.20	0.039	0.047
b	0.33	0.41	0.013	0.016
c	0.15	0.19	0.006	0.007
D	2.820	3.02	0.111	0.119
E1	1.50	1.70	0.059	0.067
E	2.60	3.00	0.102	0.118
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.60 REF		0.024 REF	
L1	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



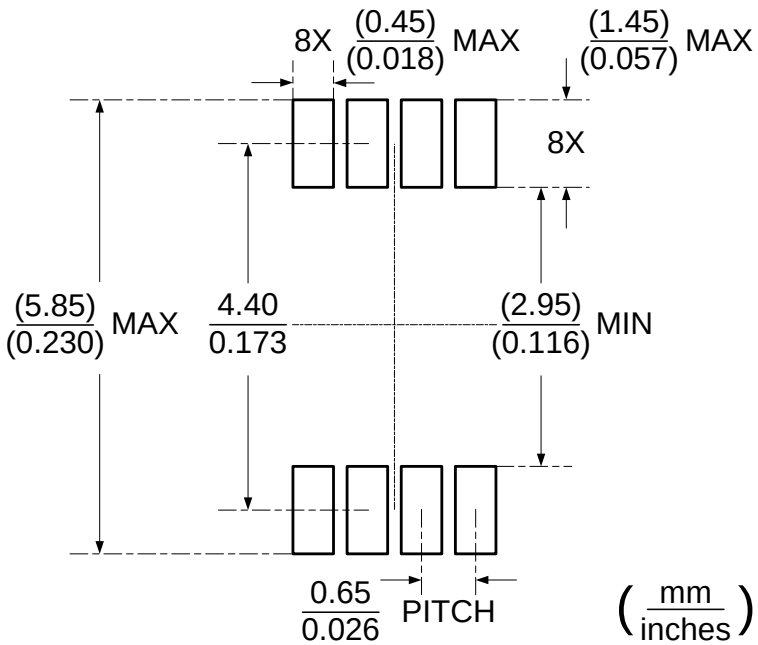
Package Outlines (continued)

DIMENSIONS, MSOP-8L



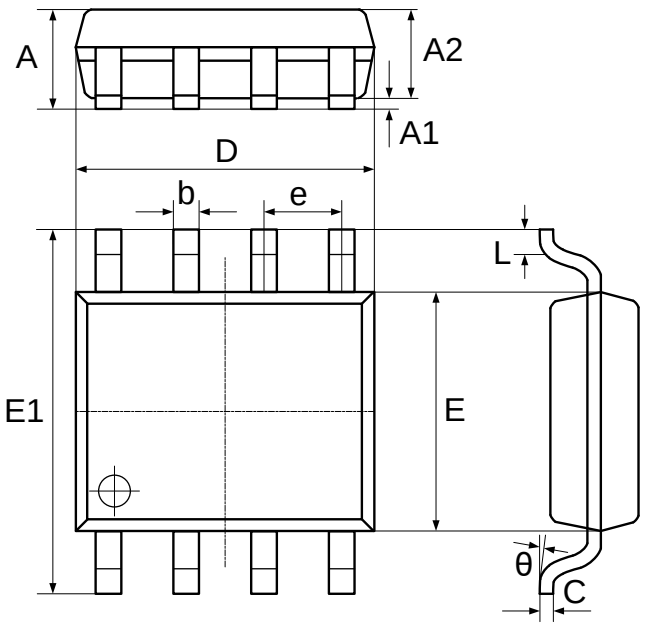
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.290	0.380	0.011	0.015
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650 TYP.		0.026 TYP.	
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



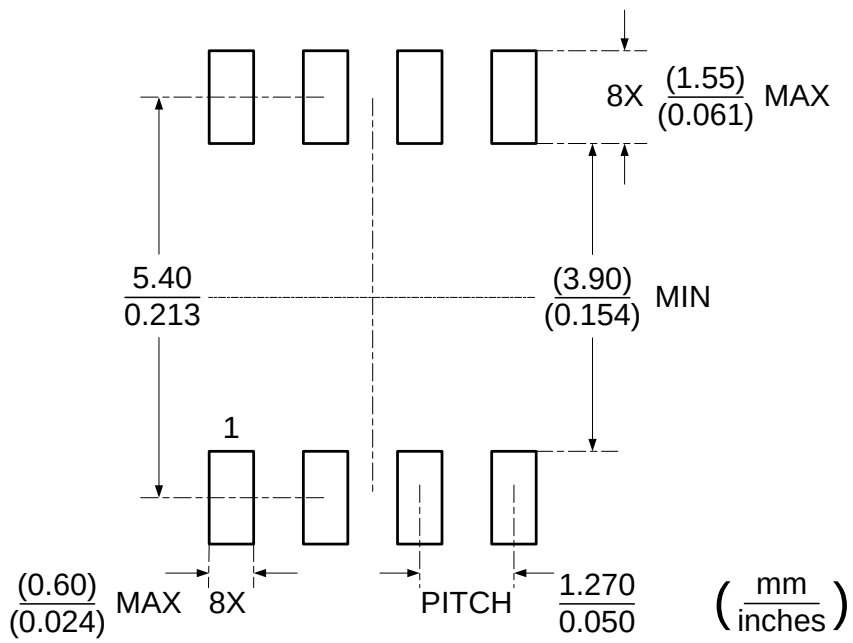
Package Outlines (continued)

DIMENSIONS, SOIC-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.054	0.066
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.051	0.059
b	0.306	0.506	0.012	0.020
C	0.203 TYP.		0.008 TYP.	
D	4.700	5.100	0.185	0.201
E	3.820	4.020	0.150	0.158
E1	5.800	6.200	0.228	0.244
e	1.270 TYP.		0.050 TYP.	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



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